# Footprint Expert Guideline

## Surface Mount and Through-hole

*by PCB Libraries, Inc.*

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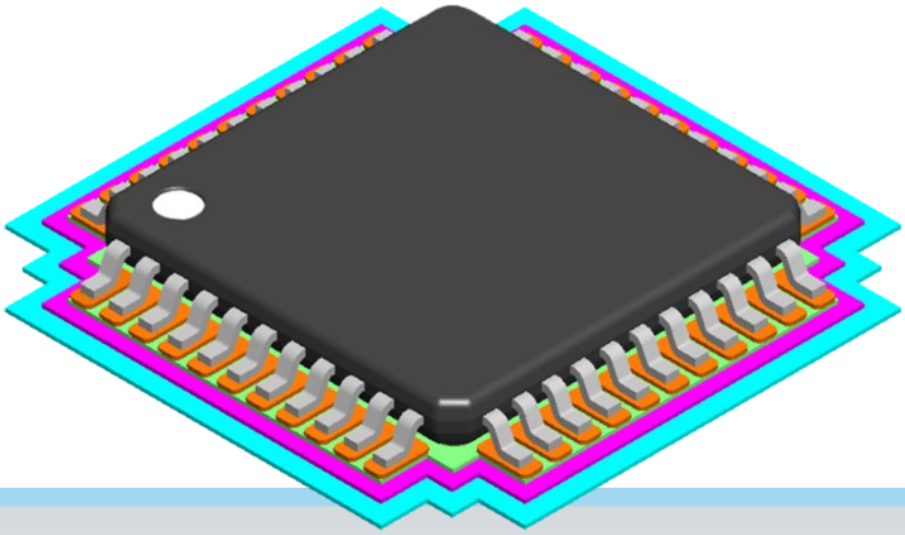

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# 1.0 – Purpose

The purpose of The Footprint Expert Guideline is to establish a comprehensive, standardized methodology for the development, naming, dimensioning, and documentation of printed circuit board (PCB) land patterns and pad stacks for both surface mount and through-hole electronic components. This guideline provides consistent rules and mathematical models for the creation of manufacturable, assembly-ready PCB footprints intended to improve design quality, interchangeability, automation, and communication throughout the electronic product development process.

This document defines terminology, density level strategies, solder joint objectives, courtyard requirements, naming conventions, drafting standards, pad stack rules, and tolerance considerations used in the generation of PCB footprints and associated library data. In addition, it provides recommended land pattern methodologies and package family definitions for a broad range of electronic component types, including surface mount, leaded through-hole, area-array, and specialized package styles.

The guideline is intended for use by PCB library developers, ECAD librarians, PCB designers, manufacturing engineers, assembly engineers, component engineers, and software systems involved in automated footprint generation and verification. The objective is to promote uniformity and repeatability in PCB land pattern creation while supporting efficient manufacturing, inspection, assembly reliability, and long-term library maintenance.

The recommendations contained within this guideline are based on accepted industry practices, mathematical modeling techniques, and practical manufacturing considerations. The information may be used independently or alongside applicable industry standards, including those published by the IPC, IEC, and FED, to support the creation of consistent and reliable PCB footprint libraries.

# 2.0 – Committee Members

This Guideline was created by PCB Libraries, with input from the committee. The individuals listed below have contributed to the development of this guideline. Company names specified below do not imply endorsement.

While all members contributed to some extent, we owe a special thanks to members who provided outstanding contribution to this guideline; such individuals are designated a ☆ star.

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# 3.0 – Terms and Definitions

**3D STEP Model**: High-fidelity, standardized files (ISO 10303) that represent the exact physical geometry of electronic components. Unlike basic 2D outlines, these "solid" models allow designers to visualize a board in three dimensions to verify mechanical fit and enclosure integration before manufacturing. 3D models can be used for Clearance & Collision Testing. They enable automated 3D Design Rule Checks (DRC) to detect if a tall capacitor will hit a lid or if a connector is properly aligned with a panel cutout. Footprint Expert autogenerates 3D STEP models for standard component families. Non-standard 3D STEP models are available for free download from the component manufacturer. STEP model names should be identical to the footprint name. The file extension is mostly .STEP but .STP is also used.

**Antipad**: The circular "no-copper" zone on a power or ground plane that surrounds a via or a plated through-hole. Without an antipad, a signal via passing through a ground plane would be permanently shorted to ground. Fabricators need this "moat" to be slightly larger than the drill size to account for small misalignments during drilling or layer registration. In high-speed designs such as PCIe or DDR4, the size of the antipad significantly affects the via's impedance. A larger antipad reduces parasitic capacitance, which helps maintain signal quality.

**Assembly Outline**: A specific mechanical layer drawing in a PCB footprint that maps the physical geometry and boundaries of a component to generate precise assembly documentation. Unlike the superficial lines found on the silkscreen layer, the assembly outline serves strictly as a back-end reference for manufacturing validation and is utilized to build Assembly Drawings rather than being printed directly onto the board surface. Assemblers cross-reference the outline to guarantee components are placed in the precise location, especially when silkscreen markings are hidden beneath a component body. Keeping the detailed component contours on a mechanical assembly layer prevents the exterior silkscreen layer from becoming cluttered or overlapping. It maps the maximum material boundaries (including tolerances) and explicitly highlights directional features, such as the location of Pin 1. The assembly outline is a closed polygon drawn to match the maximum physical dimensions of the component body. A distinct graphic indicator (such as a dot, bevel, chamfered corner or bar) mapping the location of Pin 1 or positive/negative terminals. The assembly Ref Des is located inside the assembly outline and stays there forever. Pads are normally not printed with the assembly outline, because the assembly reference designator inside the outline can cause clutter. The average line widths for the assembly outline range from 0.10 to 0.15 mm.

**Component Outline**: A closed polygon representing the nominal package outline. It has various uses depending on your footprint creation rules. It was originally intended to create an extruded 3D model without terminal leads.

**Courtyard**: A boundary layer used to define the minimum physical space a component needs on the board, including its body, pins, and a safety buffer. The courtyard is primarily for CAD design and DRC (Design Rule Check) to prevent components from being placed too close to each other. It ensures that pick-and-place machine nozzles have enough room to operate without hitting neighboring parts. It provides enough clearance for a technician to reach a component with a soldering iron or tweezers if it needs to be replaced. It prevents tall components from shadowing smaller ones, which can interfere with Automated Optical Inspection (AOI). The courtyard outline excess maps to the maximum material condition of the component package.

**Discrete Component:** A single, self-contained electronic component that performs a single, fundamental electrical function and cannot be divided into smaller individual parts. Unlike an Integrated Circuit (IC) – which combines thousands or millions of microscopic transistors, resistors, and diodes onto a single piece of silicon – a discrete component contains only one primary active or passive element inside its packaging. All discrete components are classified into one of two functional categories based on whether they require a power source to operate:

- *Passive Components:* These components cannot amplify an electrical signal or introduce net energy into a circuit. They absorb, store, or release energy:
  - ***Resistors:*** Resist the flow of electric current to control voltage and current levels. Limit current by converting electrical energy into heat.
  - ***Capacitors:*** Store energy in an electric field between their plates. When voltage changes, the electric field changes, allowing capacitors to absorb or release charge. This makes them effective for filtering, decoupling, and stabilizing power rails.
  - ***Inductors:*** Store energy in a magnetic field created by current flowing through their coil. When current changes, the changing magnetic field induces a voltage that opposes the change, allowing inductors to block high frequency noise while passing DC.

- *Active Components:* These components rely on an external power source to change, switch, or amplify electrical signals:
  - ***Diodes:*** Act as a one-way valve, allowing electrical current to flow in only one direction.
  - ***Transistors (MOSFETs & BJTs):*** Act as electronic switches or signal amplifiers, controlling a large output current with a tiny input signal.

**Footprint**: The physical layout on a circuit board that matches an electronic component's pin configuration and dimensions. It acts as a digital template that tells manufacturers exactly where to place copper pads for soldering and where to print labels for identification. A footprint contains pads, solder and paste masks, drafting outlines for silkscreen, assembly, courtyard, component, polarity marking, origin marking and terminal leads. A calculator can be used to create standard package footprints. Non-standard packages like complex connectors must use the manufacturer recommended solder pattern because there are no industry standard rules for calculating patterns.

**Keepout**: A designated "no-go" zone embedded within a component's land pattern to prevent specific design elements like copper traces, vias, or other components from being placed in a sensitive area. Unlike a courtyard, which provides a general safety margin for assembly, a keepout is often used for electrical or mechanical safety to prevent shorts, interference, or physical obstructions. Used under connectors with metal housings (like SD card holders or USB ports) to ensure traces don't run directly under sharp metal edges that could pierce the solder mask. Placed under components like crystals or oscillators to keep electrically noisy signals from passing directly beneath sensitive pins. All non-plated holes have a minimum of 0.20 mm annular ring keepout to prevent all copper features from getting near the hole.

**Land Pattern:** The specific arrangement of conductive pads or through-holes on a printed circuit board (PCB) designed to physically attach and electrically connect a specific electronic component. Created using reference documents like a manufacturer's component datasheet, a properly sized land pattern ensures solid solder joint creation, prevents manufacturing defects, and allows for optimal heat and electrical performance.

- *Anatomy of a Land Pattern:*
  - *Copper Pads (Lands):* The metal areas where component pins or balls are soldered.
  - *Solder Mask Openings:* Defines the regions cleared of insulation so solder paste can bond to the copper.
  - *Solder Paste Layer:* Dictates the layout of the stencil apertures used during machine assembly to apply paste.
  - *Silkscreen Layer:* Visible ink printed on the board indicating the outline of the part, text labels, and polarity indicators like "Pin 1".
  - *Courtyard Area:* Designated boundaries around the part ensures components are not placed too closely together, preventing physical interference during machine placement.

**Mounting Hole**: A mechanical opening drilled through a printed circuit board to secure the board physically to a chassis, enclosure, or standoff using hardware like screws, bolts, or plastic snap-rivets. Beyond mechanical retention, mounting holes are critical interface points for establishing physical earth grounding and controlling electromagnetic compatibility (EMC).

- *Plated vs. Non-Plated Mounting Holes:* Mounting holes fall into two primary mechanical styles depending on whether they interface with the board's electrical circuitry:
  - *Plated Mounting Holes (Grounded)*
    *Design:* The inner barrel of the drilled hole is electroplated with copper, which connects to a circular copper pad on the top and bottom layers. This pad is typically surrounded by a ring of exposed vias (a stitching array).
    *Function:* Used to bridge the PCB's internal ground planes directly to an external metal chassis or earth ground. The metal screw head or star washer bites into the plated pad, creating a robust, low-impedance electrical path.
    *Layout Tip:* Explicitly connect these pads to the digital ground or chassis ground net in the ECAD tool. Do not depend on the screw threads or metal hardware as the electrical path. Screws, standoffs, and metal hardware make unpredictable electrical contact. The pressure, surface oxidation, vibration, and torque all change the contact resistance. For grounding, a low impedance, repeatable path is required – mechanical joints cannot guarantee that.
    *Note:* Mounting holes also serve as key interface points for chassis grounding and EMC control. However, mechanical hardware alone must never be relied on as the primary electrical connection; grounding should always be established through intentional copper features.
- *Non-Plated Mounting Holes (Isolated)*
  - *Design:* These holes contain no copper inside the barrel or on the surrounding surface layers. They are completely unplated slots or clear drill holes.
  - *Function:* Used strictly for mechanical mounting where absolute electrical isolation from the enclosure or chassis is required.
  - *Layout Tip:* Keep a strict copper keep-out clearance zone around the edge of the hole to ensure no internal power or signal plane traces are exposed or shorted during the drilling phase of manufacturing.

**Origin Marker**: The (0,0) coordinate reference point within a component's land pattern. It serves as the "anchor" that CAD software uses to place, rotate, and move the part on the layout. More importantly, this point is exported to pick-and-place files used by assembly machines to know exactly where to drop the component. The origin for all surface mount packages should be at the geometric center (centroid) of the component. This is essential for automated pick-and-place nozzles, which grip parts by their center of gravity to prevent them from tilting or falling. The convention through-hole components are also at the center of gravity but sometimes placed at Pin 1. But placing the origin on Pin 1 when you rotate a footprint in your design tool, it pivots around the origin. If the origin is off-center, a 90° rotation will "swing" the part to a new position rather than just spinning it in place.

**Oscillator**: a surface mount (SMD) or through-hole (THD) enclosure that houses a quartz crystal alongside an internal oscillation circuit (including logic gates and load capacitors) to output a clean, standalone clock signal. Unlike bare crystals, which require external capacitors and micro-controller circuitry to oscillate, an active oscillator package only needs a stable power supply and ground to immediately output a square or sine wave.

**Pad Stack**: The total collection of features associated with a single hole or connection point on a Printed Circuit Board (PCB). A complete through-hole pad stack typically includes the drill size, the finished hole size, capture pads on both inner and outer layers, clearances for solder mask, and power planes. Surface mount pad stacks contain a pad, solder and paste masks. Pad stacks ensure reliable electrical connections and mechanical stability for soldered components.

**Package Tolerances**: Component body tolerances affect all drafting outlines including the courtyard. If the component manufacturer only provides nominal package dimensions, a 0.10 mm tolerance should be applied. Typically, the component manufacturer datasheets that provide package dimensions and tolerances, the tolerance values are sometimes too robust and unrealistic. A package tolerance larger than 0.20 mm is considered robust. Only very large component packages have tolerances greater than 0.20 mm.

The package and terminal positive and negative tolerances must be the same value. Some component manufactures tolerances are + 0.20, – 0.10. The average is +/- 0.15. If the +/- tolerances are unbalanced, the positve tolerance can be added to the Nominal dimension to calculate the Max value. The negative tolerance can be subtracted from the Nominal dimension to calculate the Min value. But then the Nominal dimension will not match the datasheet. It’s best to use a nominal +/- tolerance for all dimensions.

**Paste Mask**: Often called the solder paste, defines the specific locations and sizes of openings in a stencil used to apply solder paste to surface mount (SMD) pads. Unlike the solder mask, which is a permanent part of the board, the paste mask is a temporary tool used only during the assembly process to ensure the correct volume of solder is deposited for reflow. Paste masks are almost exclusively used for SMD components. Through-hole components typically do not have a paste mask layer because they are not soldered via the reflow process unless Pin-in-Paste technology is required.

**Photo Resist**: a photosensitive polymer used to coat printed circuit boards (PCBs). It acts as an insulating, permanent protective layer that insulates copper traces against oxidation, prevents electrical short circuits, and stops solder bridges from forming between closely spaced pads. There are two primary methods for applying a photo-imageable solder mask at home or in prototyping labs. Liquid Photo Imageable (LPI) is the industry standard and most common type. It is a liquid, UV-curable ink (often known as "green oil") that can be painted, screened, or squeegeed onto the board. Liquid Photo Imageable (LPI) conforms to the topography of the PCB traces. The silkscreen is affected by the trace bumps. Dry Film Solder Mask (DFSM) A photosensitive sheet applied using heat (via a laminator). It offers a perfectly even layer and is highly convenient for one-off designs or quick prototypes. Not recommended for mass production runs. Dry Film Solder Mask (DFSM) sits on top of PCB traces. The silkscreen is flat on the Dry Film and very legible.

**Pin-in-Paste**: Through-Hole Reflow (THR) or intrusive reflow, is a manufacturing process that allows through-hole components to be soldered using the same standard reflow oven process as surface mount devices. Instead of using a separate wave soldering machine or hand soldering for through-hole parts, solder paste is applied directly into and over the plated through-holes. A stencil prints solder paste onto the SMD pads and into the through-holes simultaneously. The entire board passes through the reflow oven. The paste melts and wicks down into the barrel of the hole, forming a solid mechanical and electrical joint.

**Polarity Marking**: Visual indicators on the silkscreen and assembly drawing layers that ensure polarized components, such as diodes, electrolytic capacitors, and ICs, are installed in the correct orientation. Proper marking is critical; installing a polarized component backward can lead to circuit failure, short circuits, or even component explosions. Components use standardized symbols to help assembly technicians and automated machines. Semiconductors use a dot to identify Pin 1. Diodes and LEDs are typically marked with a thick bar or the schematic symbol, on the assembly drawing, pointing toward the cathode (negative side). For post-assembly inspection, position markings outside the component body so they remain visible after the part is soldered. For through-hole parts, using a square pad for Pin 1 and round pads for the rest.

**Reference Designator**: A unique alphanumeric code assigned to each component on a printed circuit board (PCB). These labels serve as "geo-tags" that link the physical board to its schematic and Bill of Materials (BOM), making them essential for assembly, testing, and troubleshooting. Pick-and-place machines use these identifiers to match the correct components from the BOM to specific board coordinates. Technicians use Ref Des labels to quickly locate faulty parts described in service manuals or schematics. They ensure consistency across all design files, from the initial schematic capture to the final assembly drawing. There are normally two Ref Des designators in a footprint library, one for the silkscreen and one for the assembly drawing. The assembly Ref Des stays inside the assembly outline while the silkscreen Ref Des is placed outside the footprint and does not violate the solder mask openings.

**Semiconductor:** any solid-state electronic component – such as microprocessors, operational amplifiers, diodes, or transistors – that is mounted onto a printed circuit board to control, amplify, or switch electrical signals. In the industry, the intersection of PCBs and semiconductors focuses heavily on packaging technology, thermal management, and high-speed signal routing.

**Silkscreen Legend**: Non-conductive ink layer on a Printed Circuit Board (PCB) used to label components and provide vital information for assembly and troubleshooting. Silkscreen can include Reference Designators, Polarity Markings, Component Outline shapes that indicate where the physical component should be placed, Logos and compliance such as RoHS, CE, and FCC alongside manufacturers or brand logos. Note: silkscreen should not violate the solder mask area.

**Solder Mask**: Also known as solder resist, is the protective polymer coating applied to the copper traces of a PCB to prevent oxidation and accidental electrical shorts during assembly. It creates a non-conductive barrier that keeps molten solder confined to the pads where components are meant to be attached, effectively preventing "bridging" between closely spaced traces. Shields the copper from environmental factors like moisture, dust, and oxidation. Acts as a dielectric layer to ensure electrical isolation between signals. Prevents solder from short circuiting pads and traces during the reflow process.

**Solder Mask Web**: The terms solder mask web, solder mask sliver, and solder mask bridge all refer to the same thing: the thin strip of solder mask material that remains between two adjacent pads or mask openings. This "web" is critical because it acts as a physical dam that prevents molten solder from flowing between pads during assembly, which would otherwise cause a solder bridge (short circuit). Most PCB fabricators require a minimum web width of 0.10 mm for standard green solder mask to ensure it adheres properly without peeling off. Some fabrication shops have a minimum solder mask web of 0.075 mm. If the web is designed too thin (less than 0.075 mm), it is called a "sliver." These thin strips are prone to cracking or detaching during manufacturing, which can contaminate the board or lead to assembly failures.

**Standoff Height**: The vertical distance between the top surface of a PCB and the underside (bottom) of a mounted component. Unlike "component height," which measures to the top of the part, the standoff height defines the air gap beneath it, which is critical for cleaning, thermal management, and electrical insulation. The standoff height is used for cleaning. A minimum gap is required to allow cleaning agents to flow under components and remove flux residues after soldering. Extremely low standoffs of less than 0.03 mm can trap contaminants that lead to electrochemical migration and failure. Taller standoffs can provide better stress relief during thermal cycling, improving the long-term reliability of the joint.

**Thermal Pad**: A large metal area on the bottom of a surface mount component normally used with QFN, SON, SOP and QFP packages. It is designed to pull heat directly away from the silicon die and into the PCB. To maximize cooling, this pad must be soldered to the board. It often includes an array of thermal vias to carry heat to internal ground planes. To prevent the component from "floating" on a pool of molten solder, the paste mask should be broken into a grid of smaller windows (covering roughly 50–80% of the pad area).

**Thermal Relief**: A specialized pad connection used when a through-hole component pin connects to a large copper pour or plane. It consists of a small copper ring connected to the plane by thin "spokes". Without these spokes, a large copper plane acts as a massive heat sink during soldering, making it nearly impossible to melt the solder correctly. This often results in "cold solder joints". The spokes provide enough thermal resistance to allow for easy soldering while still maintaining a strong electrical connection.

**Terminal Leads**: Conductive pins or wires used to establish electrical connections between a printed circuit board and external components, wires, or other boards. They are categorized based on their physical style, how they secure connections, and their intended power or signal application. Through-hole terminals are round, square or rectangle. Surface Mount terminal leads are Gullwing, J-Lead, Flat, Concave, Ball, Column, End Cap (chips), Cylindrical (MELF). See chapter 12 for comprehensive explanation of all terminal leads.

**Terminal Outlines**: These outlines represent where the terminal leads to land on the pad. These outlines are an important guideline for assembly attachment QC. All terminal outlines must reside 100% on a pad for the best soldering results. If a terminal outline falls off a pad, there will be assembly attachment problems.

**Terminal Tolerances**: PCB terminal lead tolerances ensure that components can be physically inserted or placed correctly, despite small variations in component manufacturing. Terminal tolerances impact the pad stack calculations to ensure the resulting pattern will accommodate packages in the minimum, nominal and maximum material condition. However, terminal tolerances vary with the terminal lead form. Normally, the recommended terminal tolerances published in package dimensioned datasheets are slightly larger than reality.

**Varistor**: A Varistor, or surface mount device (SMD) varistor, is a voltage-dependent resistor (VDR) used to protect electronic circuits from sudden, transient overvoltages such as electrostatic discharge (ESD) and lightning-induced surges. It acts as a safety device by automatically diverting excess current away from sensitive components.

- *Function and Operation:* The name "varistor" is a combination of "variable" and "resistor", accurately describing its core function.
  - *High Resistance (Normal Operation):* Under normal operating voltage, a chip varistor has very high resistance, behaving almost like an open circuit and allowing only a negligible leakage current to flow.
  - *Low Resistance (Surge Event):* When a voltage surge exceeds a specific threshold voltage (known as the varistor voltage or clamping voltage), the varistor's internal resistance drops dramatically.
  - *Voltage Clamping:* This rapid drop in resistance allows the varistor to conduct the large surge current safely to ground or another part of the circuit, effectively "clamping" the voltage to a safe level and protecting downstream components.
  - *Bidirectional Protection:* Unlike Zener diodes, most varistors are bidirectional and can suppress voltage spikes in both positive and negative directions, making them suitable for both AC and DC circuits.
- *Construction:* Varistors are typically multilayer ceramic devices made from zinc oxide (ZnO) material pressed between metal electrodes using a multilayering process. The numerous grain boundaries within the ceramic material provide the non-linear voltage-current characteristics.
- *Key Characteristics*
  - *Fast Response Time:* Chip varistors react very quickly to surges, often within nanoseconds (300 to 700 picoseconds), suppressing the overvoltage before it reaches its peak.
  - *Compact Size:* As SMD components, they have a small footprint, enabling installation in miniature and high-density electronic devices.
  - *Noise Suppression:* They inherently possess some capacitance and can offer noise suppression effects, sometimes replacing a combination of a TVS diode and a capacitor for EMI filtering in a single component.
- *Applications:* Varistors are widely used across various electronic sectors for circuit protection.
  - *Consumer Electronics:* Found in smartphones, computers, and tablets for ESD protection on I/O ports, buttons, and connecting terminals.
  - *Automotive Electronics:* Protect sensitive control units (ECUs) and communication buses (CAN, LIN) from voltage spikes and surges generated by ignition systems or inductive loads.
  - *Power Supplies:* Installed in AC power supplies and adapters to guard against surges from the main power line.
  - *Industrial Equipment:* Protect control panels, motors, and automation systems from switching surges and electrical noise.

**Voltage Regulator:** An active electronic component that accepts a variable or unstable input voltage and outputs a steady, precise, and clean voltage regardless of changes to load current or input supply fluctuations. They are fundamental to power management on any PCB, ensuring sensitive digital ICs, microcontrollers, and analog sensors receive safe, predictable power rails.

**Zero Orientation**: The default "0-degree" rotational angle for a component's footprint in a CAD library. It ensures that automated pick-and-place (PnP) machines interpret centroid data (X-Y-Rotation files) consistently, regardless of how a component was originally drawn. The industry follows two primary standards for defining where Pin 1 is located when a part is at zero rotation. IPC-7351B has Pin 1 is in the upper-left corner for multi-pin components. This was a complete change from the IPC-SM-782 standard that was the leading document for 18 years since 1987. IPC-7351 replaced IPC-SM-782 in 2005. In 2007 the IEC 61188-7 Standard was released with Pin 1 is in the lower-left corner. Pin 1 Lower Left is the default Zero Component Orientation in Footprint Expert.

## 3.1 Component Descriptions

**Antenna:** An antenna is a compact, surface mountable electronic component designed to transmit and receive high-frequency radio waves in wireless devices. Valued for their small footprint, low profile, and cost-effectiveness, they are ideal for space-limited applications such as smartphones, wearable devices, and Wi-Fi routers.

- *Design and Function:* Antennas function by creating a standing wave of an electrical field within a ceramic dielectric material (which has a high permittivity), allowing them to resonate at specific frequencies while being much smaller than traditional antennas designed for the same wavelength in free space.
    - *Construction:* They are typically manufactured using Low-Temperature Co-fired Ceramic (LTCC) technology, integrating metal layers within a ceramic body.
    - *Ground Plane Dependency:* Chip antennas are dependent on the device's printed circuit board (PCB) ground plane to form a complete resonant circuit and achieve optimal performance.
    - *Impedance Matching:* To ensure maximum power transfer and efficiency, a matching network (often a Pi-network with capacitors and inductors) is used to optimize the impedance between the antenna and the radio frequency (RF) circuit.
    - *Performance Factors:* The antenna's performance is highly influenced by its placement, the size and shape of the PCB ground plane, the device's enclosure (especially metal components), and the presence of nearby components.

**Capacitor:** A capacitor, also known as a surface mount or through-hole device, is an electronic component that stores electrical energy. These components are designed to be mounted directly onto the surface of printed circuit boards (PCBs), enabling the miniaturization and high integration of modern electronic devices like smartphones and computers.

- *Function and Operation:* The primary function of a capacitor is to store electrical charge. This is achieved by using two conductive plates separated by an insulating material called a dielectric.
- *Energy Storage:* When a voltage is applied, charges build up on the plates, creating an electric field across the dielectric. The amount of charge stored is proportional to the applied voltage and the component's capacitance.
- *AC vs. DC:* Capacitors block the flow of direct current (DC) once charged, but allow alternating current (AC) signals to pass through, a key property used in filtering and coupling applications.
- *Rapid Charge/Discharge:* Unlike batteries, which store energy chemically, capacitors store energy physically in an electric field, allowing them to charge and discharge extremely quickly.
- *Filtering:* In power supplies, capacitors act as reservoirs, smoothing out voltage fluctuations (ripples) by charging during voltage peaks and discharging during valleys, ensuring a stable DC output.
- *Common Types of Capacitors:* Chip capacitors come in various types, primarily differentiated by their dielectric material, which determines their characteristics and suitability for different applications.
- *Multilayer Ceramic Chip Capacitors (MLCCs):* The most common type, MLCCs use alternating layers of ceramic and metal electrodes.
  *Features:* Non-polarized (can be connected in either direction), wide range of capacitance values, high frequency performance, and low Equivalent Series Resistance (ESR).
    - *Dielectrics:* Common ceramic dielectrics have specific temperature characteristics, such as NP0 (C0G) for high stability or X7R/X5R for higher capacitance in a smaller size, though with less temperature stability.
- *Tantalum Chip Capacitors:* These polarized capacitors offer high capacitance per unit volume in a compact, stable package.
  *Features:* Used in applications where high reliability and high capacitance in a small size are needed, such as in portable electronics and military systems. They are sensitive to overvoltage and require correct polarity during installation.
- *Aluminum Electrolytic Chip Capacitors:* Polarized components that provide very high capacitance values.
  *Features:* Larger physically than ceramic or tantalum chips for the same capacitance, typically used in low-frequency power supply filtering applications for smoothing voltage.
- *Polymer Capacitors:* Use a solid conductive polymer as the electrolyte, offering very low ESR and stable performance over a wide temperature range, making them ideal for high-speed, high-efficiency power supply circuits in modern computing.
- *Decoupling & PDN Impedance Control:* In high-speed digital systems, MLCC capacitors are used as decoupling elements to lower the Power Distribution Network (PDN) impedance across a wide frequency range. When placed the power and ground planes, they supply fast transient currents and suppress voltage droop caused by rapid switching events. Their effectiveness depends on minimizing loop inductance, which is influenced by pad geometry, via placement, and mounting style. Arrays of MLCCs with different capacitance values are used to maintain PDN impedance below the system's target impedance, ensuring stable power delivery for processors, FPGAs, and high-speed memory interfaces.

**Choke**: A compact, surface mount device (SMD) inductor specifically designed to block or "choke" high-frequency alternating currents (AC) while allowing direct current (DC) or low-frequency signals to pass with minimal resistance. They are essential for filtering noise and protecting sensitive circuits in modern electronics.

- *Design and Function:* Chokes operate on the principle of inductance: when current flows through the winding, it creates a magnetic field. Any attempt to change that current causes the magnetic field to change, and this changing magnetic field induces an electric field (a voltage) that opposes the change. The result is that the choke presents low impedance to steady DC, but increasingly high impedance as the frequency of the AC component rises.
    - *Construction:* Chip chokes consist of a coil of insulated wire wound around a core material, typically a ceramic (air core) or a magnetic material like ferrite. The core material increases the inductance within a small physical volume.
    - *Filtering:* By placing a choke in series with a power line or signal path, it effectively blocks unwanted high-frequency noise (like electromagnetic interference, EMI) from reaching sensitive components while allowing the desired low-frequency or DC power/signal to proceed.
    - *Energy Storage:* Chokes store energy temporarily in their magnetic field. This property is particularly useful in power supplies for smoothing out voltage and current fluctuations, creating a more stable output.
- *Key Characteristics*
    - *Impedance vs. Frequency:* The key characteristic is that their impedance increases with frequency, which is why they are effective at blocking high-frequency noise.
    - *Low DC Resistance:* They are designed to have low DC resistance (DCR) to minimize power loss and heat generation during normal operation.
    - *Compact Size:* As chip (SMD) components, they have a small footprint, enabling dense circuit board designs common in portable devices.
    - *Types:*
        - *Radio Frequency (RF) Chokes:* Block radio frequencies while passing audio and DC.
        - *Common Mode Chokes:* Built with two magnetically coupled windings, common mode chokes present high impedance to common mode currents while allowing differential mode signals to pass with minimal distortion. They suppress EMI generated when imperfections in a differential pair (such as trace imbalance, skew, connector asymmetry, or component tolerances) cause differential to common mode conversion. This converted common mode energy is a major source of radiated emissions on high-speed interfaces such as USB, HDMI, Ethernet, and CAN Bus. By blocking the unwanted common mode component while leaving the intended differential signal untouched, the choke improves signal integrity and reduces system level EMI.

- *Applications:* Chokes are vital in modern electronics for ensuring clean power delivery and signal integrity.
    - *Power Supplies:* Used in switching power supplies to smooth out the rectified DC output and prevent high-frequency switching noise from feeding back into the main power line.
    - *Automotive Electronics:* Protect sensitive systems from voltage spikes and filter noise within vehicle networks (like CAN-Bus).
    - *Data Lines:* Common mode chokes are essential for maintaining signal integrity on high-speed differential signal lines (USB, Ethernet) by suppressing noise without attenuating the actual signal.
    - *RF Systems:* Found in communication devices, antennas, and oscillators to prevent unwanted high-frequency signals from interfering with circuit operations.

**Crystal**: A chip crystal, in electronics, refers to a compact, surface mount device (SMD) component used to generate highly stable and precise timing signals, which act as the "heartbeat" or clock for most digital circuits. These components come in two main forms: *crystal resonators* and *crystal oscillators*.

- *Function and Operation:* The operation of chip crystals relies on the piezoelectric effect, a property of certain materials, most commonly synthetic quartz.
    - *Piezoelectric Effect:* When an electrical voltage is applied across a quartz crystal, it physically deforms or vibrates at a specific natural frequency. Conversely, mechanical stress on the crystal generates a voltage.
    - *Resonance:* The crystal's physical dimensions (size, shape, and how it is cut) determine its natural resonant frequency.
    - *Signal Generation:* In a circuit, the crystal is placed between electrodes. An external circuit (amplifier and capacitors) sustains these vibrations, converting the mechanical resonance back into a stable, continuous electrical signal. This results in a highly accurate frequency, often measured in parts per million (ppm), which is far superior to other timing methods.

- *Types of Chip Crystals:* The main distinction is between passive components that require external circuitry and active components that are integrated solutions.
  - *Crystal Resonators (Passive Crystal)*
    A simple quartz crystal chip with two pins, housed in a sealed metal can or ceramic package.
    *Function:* Requires an external oscillator circuit (typically including resistors and capacitors) on the PCB to generate a clock signal.
    *Characteristics:* Cost-effective, simple, but the final frequency stability depends on the matching of external components.
  - *Crystal Oscillators (Active Crystal)*
    A complete timing circuit in a single surface mount package, typically with four pins.
    *Function:* Contains both the crystal unit and the necessary internal oscillator circuitry, allowing it to generate a stable frequency signal (usually a CMOS square wave) simply by applying power.
    *Characteristics:* Offers higher stability and accuracy because the crystal and circuit are perfectly matched by the manufacturer.
- *Applications:* Due to their precision and stability, chip crystals are indispensable in nearly all modern electronic devices.
  *Computing:* Provide the essential clock signals for microcontrollers, CPUs, and microprocessors to synchronize all internal operations and data transfers.
  *Communication Systems:* Generate stable reference frequencies for radio transmitters and receivers (Wi-Fi, Bluetooth, 5G networks, satellite communication), ensuring data integrity and synchronization.
  *Timekeeping:* Found in digital watches, clocks, and real-time clocks (RTCs) to keep track of time with high accuracy over long periods.
  - *Test and Measurement Equipment:* Used in precision instruments where timing accuracy is paramount.
  - *Embedded Systems:* Integrated into IoT devices, automotive systems, and medical equipment (like pacemakers and MRI machines) where reliable timing is critical for operation.

**Diode**: A chip diode, also known as a surface mount device (SMD) diode, is a miniature semiconductor component that acts as a one-way valve for electric current, allowing it to flow in only one direction (from the anode to the cathode) while blocking it in the reverse direction. They are a fundamental building block in modern, compact electronic circuits.

- *Function and Operation:* Diodes work based on a p-n semiconductor junction, which has low resistance in the forward direction and high resistance in the reverse direction.
  - *Unidirectional Current Flow:* The primary function is to enforce a one-way flow of current, which is essential for managing power and protecting sensitive components from reverse polarity or voltage spikes.
  - *Forward Bias:* When a positive voltage is applied to the anode relative to the cathode (forward bias), the diode allows current to pass easily once the voltage exceeds a small forward voltage drop (around 0.7V for silicon diodes, less for Schottky diodes).
  - *Reverse Bias:* When voltage is applied in the reverse direction (cathode more positive than anode), the diode acts as an insulator and blocks the current flow. This state is maintained until a large enough reverse voltage (breakdown voltage) is reached, at which point current will suddenly flow and potentially damage the diode, unless it is a specialized Zener or TVS diode.
- *Common Types of Diodes and Applications:* Diodes are available in various types, each optimized for specific functions and packaged in compact surface mount formats (e.g., SMA, SMB, SMC, SOD-123).
  - ***Rectifier Diodes***
    *Function:* Convert alternating current (AC) into pulsating direct current (DC).
    *Applications:* Found in power supplies, AC adapters, and battery chargers to provide the necessary DC power for electronic devices.
  - ***Schottky Diodes***
    *Function:* Characterized by a metal-semiconductor junction, offering a very low forward voltage drop and extremely fast switching speeds.
    *Applications:* Ideal for high-frequency applications, switching power supplies, and polarity protection circuits where efficiency and speed are critical.
  - ***Zener Diodes***
    *Function:* Designed to operate reliably in the reverse breakdown mode, maintaining a stable, constant voltage across their terminals once a specific "Zener voltage" is reached.
    *Applications:* Used for voltage regulation, creating a stable voltage reference in circuits, and protection against overvoltage conditions.

- ***TVS (Transient Voltage Suppression) Diodes***
  *Function:* Engineered to quickly respond to and absorb high-energy voltage spikes (transients) in nanoseconds.
  *Applications:* Essential for protecting sensitive integrated circuits (ICs), data lines (like USB), and power lines from electrostatic discharge (ESD) and power surges.

**Ferrite Bead**: A chip ferrite bead is a surface mount passive component used as a low-pass filter to suppress high-frequency noise, specifically *Electromagnetic Interference (EMI)* and *Radio Frequency Interference (RFI)*, in electronic circuits. It works by absorbing unwanted high-frequency energy and dissipating it as a small amount of heat.

- *Function and Operation:* Unlike a standard inductor which stores energy in a magnetic field, a ferrite bead is engineered to be a frequency-dependent resistor.
  - *Noise Suppression:* It is placed in series with a power or signal line to block differential mode noise.
  - *Energy Conversion:* The ferrite material's magnetic properties cause the high-frequency noise signal's energy to be converted into thermal energy (heat), effectively filtering out the interference.
  - *Frequency Dependence:* At low frequencies (DC or desired signal frequencies), the ferrite bead has a very low impedance (low DC resistance), allowing the signal or power to pass through with minimal impact. As the frequency increases into the noise spectrum, its impedance increases significantly, primarily due to its resistive properties, thereby blocking the noise.
- *Key Characteristics*
  - *Construction:* Chip ferrite beads are made from a ceramic compound composed of iron, nickel, and zinc oxides, typically using multilayer construction techniques.
  - *Impedance Profile:* Datasheets for ferrite beads show an impedance (Z) versus frequency graph, highlighting inductive (X) and resistive (R) components. For optimal noise filtering, the bead should be selected so that its resistive component is maximized at the specific noise frequency requiring attenuation.
  - *DC Bias Effect:* The performance of a ferrite bead is highly dependent on the DC current flowing through it. Applying a large DC current can saturate the ferrite material, significantly reducing its impedance and filtering effectiveness. Designers often operate them at about 20% of their rated current to maintain performance.
  - *Combination with Capacitors:* Ferrite beads are often paired with decoupling capacitors to form a low pass filter. The bead absorbs high frequency magnetic field energy, while the capacitor shunts high frequency electric field energy to ground. Together they reduce a wider range of power supply noise than either component alone.
- *Applications:* Ferrite Beads are widely used to ensure electromagnetic compatibility (EMC) and improve signal integrity in sensitive electronic devices.
  - *Power Supply Lines:* Suppressing high-frequency switching noise from DC-DC converters and power rails.
  - *Signal and Data Lines:* Cleaning noise on general signal lines and high-speed data interfaces like USB and HDMI to prevent data corruption or interference (autointoxication).
  - *Integrated Circuit Protection:* Placed near the pins of integrated circuits to suppress parasitic oscillations and enhance circuit reliability.
  - *Automotive and Medical Equipment:* Used in systems where reliable operation and freedom from interference are critical for safety and performance.

**Filter**: A chip filter, typically a surface mount device (SMD), is an electronic component or an integrated circuit (IC) designed to selectively pass signals of certain frequencies while blocking or attenuating others. They are critical for managing the flow of electrical signals and reducing unwanted noise in modern, compact electronic systems.

- *Function:* A filter shapes a signal by controlling how electric and magnetic fields move through a circuit. Capacitors respond to changes in the electric field, inductors respond to changes in the magnetic field, and resistive or lossy elements absorb field energy. By combining these behaviors, filters pass some frequencies while attenuating others.
  - *Signal Integrity:* The primary role is to improve signal quality by removing noise or isolating specific frequency bands, which is essential for systems like audio processing and radio communications.
  - *Frequency Management:* They define a "passband" (frequencies allowed through) and a "stopband" (frequencies blocked), shaping the frequency response of a circuit.
  - *Miniaturization:* Chip filters, whether discrete passive components (like an LC filter combining an inductor and capacitor on a single chip) or complex integrated circuits, enable dense circuit board designs with improved performance and reduced parasitic effects compared to larger, through-hole components.

- *Types of Filters:* Filters are classified based on the frequency range they affect and their internal design (active or passive).
  - *By Frequency Response:*
    *Low-Pass Filter:* Passes low-frequency signals and blocks higher frequencies (e.g., in power supplies to smooth DC voltage).
    *High-Pass Filter:* Passes high-frequency signals and blocks lower frequencies (e.g., in communication systems to block DC bias).
    *Band-Pass Filter:* Passes only a specific range of frequencies while blocking those above and below (e.g., in radio tuners to select a specific station).
    *Band-Stop (Notch) Filter:* Blocks a specific range of frequencies but allows all others to pass (e.g., to eliminate specific interference or hum).
  - *By Design Type:*
    *Passive Filters:* Built using only resistors, capacitors, and inductors; they don't require an external power source and generally have simple designs.
    *Active Filters:* Incorporate active components like operational amplifiers (op-amps) along with resistors and capacitors to provide signal amplification and improved stability, typically used for lower frequencies.
    *Integrated Circuit (IC) Filters:* Full filter circuits integrated into a single semiconductor chip, often including advanced designs like Butterworth or Chebyshev responses.
- *Applications:* Filters are fundamental to virtually all non-trivial electronic systems.
  - *Audio Systems:* Used for tone control, speaker crossover networks, and noise reduction.
  - *Communication Devices:* Essential for channel selection, signal separation in 5G networks, Wi-Fi, and Bluetooth, ensuring clean data transmission.
  - *Power Electronics:* Suppress voltage spikes, reduce electromagnetic interference (EMI), and smooth power supplies. For example, a *Murata BNX02 SMD EMI Filter* is an LC combined filter used to suppress noise in automotive applications.
  - *Data Processing:* Placed in front of analog-to-digital converters (ADCs) to reduce aliasing and ensure signal integrity.

**Fuse:** A Fuse is a miniature, surface mount device (SMD) designed to protect electronic circuits from damage caused by excessive current. They are essential safety devices that interrupt the flow of electricity when current exceeds a predetermined limit, preventing damage to downstream components and potential fire hazards.

- *Function and Operation:* The operation of a fuse is based on the heating effect of current. It contains a precise metallic or thin-film conductive element designed to melt and break the circuit when subjected to overcurrent conditions.
  - *Normal Operation:* Under normal current flow, the fuse element generates a small amount of heat that is efficiently dissipated, allowing the circuit to operate normally.
  - *Overcurrent Event:* If the current suddenly surges beyond the fuse's rated ampere limit (due to a short circuit or overload), the increased heat causes the internal element to quickly reach its melting point and melt (or "blow").
  - *Circuit Interruption:* The melting of the element creates an open circuit, instantly stopping the flow of current and isolating the power source from the delicate components it protects.
  - *Single-Use vs. Resettable:* Traditional single-use chip fuses must be replaced after they blow. Resettable chip fuses (PPTC or polymeric positive temperature coefficient fuses) use a polymer material that temporarily changes to a high-resistance state when overheated, and then resets once the fault is cleared and the component cools down.
- *Types of Fuses:* Fuses are primarily categorized by their response speed to overcurrent events:
  - *Fast-Acting Fuses:* These are designed to blow very quickly in response to overcurrent conditions and are suitable for protecting components that are highly sensitive to overcurrent, such as integrated circuits.
  - *Slow-Blow (Time-Delay) Fuses:* These are designed with a time delay to withstand transient inrush currents or momentary surges that occur when equipment is first powered on (common in circuits with motors or large capacitors), but still interrupt the circuit during a prolonged overload.
- *Applications:* The ultra-compact size and reliability of chip fuses make them a standard component in modern, high-density electronics.
- *Common applications include:*
  - *Consumer Electronics:* Smartphones, laptops, digital cameras, and game consoles.
  - *Power Management:* Protecting lithium-ion battery packs and DC-to-DC converters.
  - *Automotive Electronics:* Safeguarding sensitive in-car circuits from voltage spikes and overcurrent conditions.
  - *Industrial and Medical Devices:* Used where space efficiency and reliability, precise protection are mandatory for safety and performance.

  When selecting a fuse, designers must consider factors such as the normal operating current, maximum voltage rating, fusing current, and specific time-current characteristics to ensure optimal protection for the circuit.

**Inductor:** Store energy in a magnetic field created by current flowing through their coil. When the current changes, the changing magnetic field induces a voltage that opposes the change. This makes inductors pass DC easily while resisting high frequency signals, allowing them to block or filter unwanted RF noise.

- *Function and Operation:* Inductors work by storing energy in a magnetic field created when current flows through a coil. Any change in the current forces the magnetic field to change, and the changing field induces a voltage that opposes the change.
  - *Opposing Current Changes:* When current rises, the expanding magnetic field induces a voltage that pushes back against the increase. When current falls, the collapsing field releases its stored energy, trying to keep the current flowing. This field driven opposition is what gives inductors their stabilizing behavior.
  - *Filtering (Choke Function):* Because high frequency signals cause rapid magnetic field changes, inductors generate strong opposing voltages at high frequencies. This makes them effective at blocking high frequency noise while passing DC and slow variations.
  - *Energy Storage:* The magnetic field itself stores energy, which can be released back into the circuit. This property is essential in DC DC converters and other power processing circuits.
  - *Impedance:* An inductor's impedance increases with frequency because faster current changes create stronger induced voltages. This frequency dependent behavior is the basis for tuning and filtering applications.
- *Types of Inductors:* Inductors are manufactured using various techniques to optimize performance for specific frequency ranges and power requirements.
  - *Wire-Wound Type:*
    A fine insulated wire is wound around a core material, often ceramic or ferrite.
    *Characteristics:* Known for a wide range of inductance values, high quality factors (Q), and high current handling capacity.
    *Applications:* Used in RF circuits and power circuits where high performance is needed.
  - *Multilayer (Laminated) Type:*
    Made by alternate printing and laminating layers of ferrite or ceramic material with conductive patterns to form an internal coil with a closed magnetic circuit.
    *Characteristics:* Very small, excellent magnetic shielding (reduces interference with neighboring components), suitable for high-density installation.
    *Applications:* Common in mobile phones, wireless LANs, and high-frequency digital signal processing equipment due to their compact size and good high-frequency characteristics.
  - *Film Type:*
    Created using thin-film deposition technology, with electrodes concentrated on a single layer.
    *Characteristics:* Offers high precision, high stability, and maintains a high Q value in the microwave frequency band.
    *Applications:* Suited for highly precise high-frequency and microwave applications where stability is critical.
- *Applications:* Inductors are integral to modern electronic design.
  - *Power Management ICs:* Used in DC-DC converters and voltage regulators for voltage conversion, filtering, and energy storage.
  - *RF (Radio Frequency) Circuits:* Essential in wireless communication devices, transceivers, and antennas for signal processing, impedance matching, and filtering at high frequencies.
  - *Signal Filtering:* Used with capacitors to form LC filters, which isolate and filter AC signals and reduce unwanted noise in signal lines.
  - *Resonant and Timing Circuits:* Paired with capacitors and resistors to form tuning or oscillator circuits that generate precise frequencies for system clocks and radio tuning.
  - *Data Lines:* Common mode chip inductors are used on high-speed data lines (USB 2.0, HDMI, LVDS) to suppress common-mode noise without distorting the high-speed signal transmission.

**LED:** A LED, also known as a surface mount device (SMD) LED, is a compact electronic component that emits light when an electric current passes through it. These are the core light-generating units in modern lighting and display technologies, valued for their small size, high efficiency, and versatility.

- *Function and Operation:* LED stands for Light Emitting Diode, and its operation is based on the principles of semiconductors.
  - *Electroluminescence:* The core of the chip LED is a semiconductor chip (or die) made of materials like gallium nitride or gallium phosphide. This chip contains a p-n junction.
  - *Current Flow:* When a voltage is applied in the forward direction (positive to anode, negative to cathode), electrons and "holes" (positive charge carriers) are pushed toward the junction.
  - *Photon Emission:* The electrons and holes recombine at the junction, releasing energy in the form of photons (light). The color of the light produced depends on the specific semiconductor materials used.

- *Packaging:* The semiconductor chip is typically encased in a plastic or ceramic package that protects it from damage and helps to focus the light output. A phosphor layer is often used with a blue-light emitting chip to create white light.
- *Common Types of LEDs:* LEDs are often identified by a four-digit number that indicates their physical dimensions in millimeters (e.g., a 5050 chip is 5.0mm x 5.0mm).
  - ***SMD (Surface-Mounted Device) LEDs**:* The most common type, these are individual chips soldered directly onto the PCB. They are highly versatile and can contain multiple diodes (e.g., three diodes in a 5050 package to create RGB color mixing).
  - ***COB (Chip-on-Board) LEDs**:* Multiple small LED chips (often nine or more) are packed closely together on a single substrate to form a lighting module.
  - *Features:* Provides high light intensity, a uniform light appearance (less glare), and good thermal management due to direct mounting on a heat-conducting substrate.
  - *Applications:* Used in high-power applications like floodlights, street lights, and downlights.
- *Applications:* The compact size, high efficiency, and durability of chip LEDs make them suitable for a vast array of applications across many industries.
  - *Consumer Electronics:* Used for display backlighting in smartphones, tablets, and TVs, as well as indicator lights in various gadgets and wearables.
  - *General Illumination:* Widely employed in residential, commercial, and industrial lighting, including household bulbs, office panels, and street lighting.
  - *Automotive Lighting:* Integrated into headlights, taillights, interior lighting, and dashboard indicators due to their reliability and low power consumption.
  - *Horticulture and Medical:* Specialized chip LEDs emitting specific wavelengths are used in grow lights to optimize plant growth and in surgical lighting where precision is critical.
  - *Displays and Signage:* Form the pixels in large LED walls and digital billboards, delivering high visibility and vivid colors.

**Resistor**: A Resistor, also known as a surface mount device (SMD) resistor, is a small electronic component used in circuits to control current flow, divide voltage, or terminate signals. Unlike larger through-hole resistors, they mount directly onto a printed circuit board (PCB), allowing for more compact designs and automated manufacturing.

- *Function and Operation:* Chip resistors operate based on Ohm's Law, using a resistive element to oppose electrical current. Their functions include:
  - *Current Limiting:* Used in series with components like LEDs to protect them from excessive current.
  - *Voltage Dividing:* Connecting resistors in series can create a lower, proportional voltage.
  - *Current Detection:* By measuring voltage drop across a low-resistance chip resistor, current can be monitored.
  - *Biasing:* Providing necessary voltage levels to semiconductor components for proper operation and signal conditioning.
- *Types of Chip Resistors by Technology:* Resistors are typically made using two main methods, each with different properties:
  - *Thick Film Resistors:* These use a resistive paste screen-printed onto a ceramic base. They are common, cost-effective, and suitable for general uses where high precision is not essential.
  - *Thin Film Resistors:* These involve depositing a very thin metallic layer onto an insulating material. They offer higher precision, better stability, tighter tolerances, and lower noise but are more expensive. They are used in sensitive applications like medical equipment and scientific instruments.

**Thermistor**: A Thermistor is a surface mount device (SMD) that acts as a thermally sensitive resistor, changing its electrical resistance in response to temperature changes. They are essential for temperature sensing, control, and circuit protection in compact modern electronics.

- *Function and Operation:* The term "thermistor" is a blend of "thermal" and "resistor". They are typically made from a pressed and sintered mixture of metal oxides (like manganese, nickel, cobalt, and iron oxides) and coated in materials like epoxy or glass for protection. Chip thermistors are generally integrated into a voltage divider circuit to convert the resistance change into a measurable voltage signal that can be interpreted as a temperature reading.
- *Types of Chip Thermistors:* The two main categories of thermistors are defined by their temperature coefficient:
  - ***NTC (Negative Temperature Coefficient) Thermistors**:* The resistance decreases as the temperature increases.
    - *Primary Use:* Temperature measurement, sensing, and compensation (e.g., in digital thermometers, thermostats, HVAC systems, and battery management systems). They are also used as inrush current limiters, presenting high initial resistance that drops as they heat up during normal operation.
  - ***PTC (Positive Temperature Coefficient) Thermistors**:* The resistance increases as the temperature increases.
    - *Primary Use:* Circuit protection and self-regulating heaters. When the current becomes excessive and the thermistor heats up, its resistance rapidly increases, limiting the current flow and acting as a resettable fuse.

- *Applications:* Due to their high sensitivity and fast response time within specific temperature ranges, chip thermistors are used in numerous applications.
  - *Temperature Measurement:* Monitoring engine coolant or oil temperature in automotive systems.
  - *HVAC Systems:* Regulating temperature in air conditioners and refrigerators.
  - *Consumer Appliances:* Found in coffee makers, hair dryers, and toasters for precise temperature control.
  - *Circuit Protection:* PTC types are used to protect sensitive telecom apparatus and motors from overcurrent.
  - *Medical Devices:* Used in applications requiring precise temperature control and monitoring.

# 4.0 – Three-Tier Density Levels

Performance classification: IPC J-STD-001, formally titled "Requirements for Soldered Electrical and Electronic Assemblies," is the global industry standard for soldering materials and processes. Unlike other standards that focus solely on visual inspection, J-STD-001 emphasizes **process control**, ensuring that the assembly is built correctly from the start.

- **Materials & Equipment**: Specifies acceptable types of solder (both leaded and lead-free), flux, adhesives, and tools like soldering irons or rework stations.
- **Soldering Processes**: Covers methods for manual, wave, and reflow soldering, including specific requirements for component mounting and hole fill.
- **Verification & Cleaning**: Defines cleanliness testing and inspection methodology to ensure assemblies are free from harmful contaminants.

**Classification**: Products are divided into three classes based on their criticality:

**CLASS 1 General Electronic Products**
Includes products suitable for applications where the major requirement is function of the completed assembly.

**CLASS 2 Dedicated Service Electronic Products**
Includes products where continued performance and extended life are required, and for which uninterrupted service is desired but not critical. Typically, the end-use environment would not cause failures.

**CLASS 3 High Performance Electronic Products**
Includes products where continued high performance or performance-on-demand is critical, equipment downtime cannot be tolerated, end-use environment may be uncommonly harsh, and the equipment must function when required, such as life support or other critical systems.

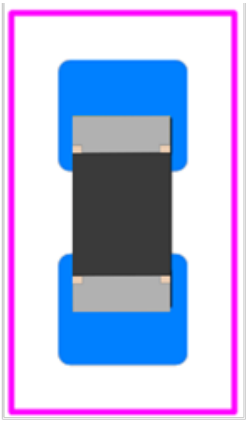
The use of performance classes (**1**, **2**, and **3**) is combined with that of component density levels (**A**, **B**, and **C**) in explaining the condition of an electronic printed board assembly.

As an example, combining the description as Levels **1A** or **3B** or **2C**, would indicate the different combinations of performance and component density to aid in understanding the environment and the manufacturing requirements of a particular printed board assembly.

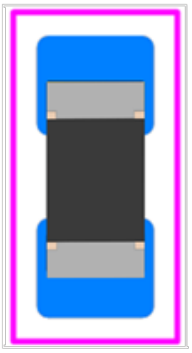
**The Three Density Levels**

- **Density Level A: Maximum (Most) Land Protrusion**
  - IPC Designation: **M** (for Maximum footprint).
  - Characteristics: Provides the largest Pad size and Courtyard area and most robust solder joints.
  - Applications: Suitable for prototypes, low-density boards, or products subjected to high shock or vibration. It offers a wider "process window," making it the most rework-friendly level.
- **Density Level B: Median (Nominal) Land Protrusion**
  - IPC Designation: **N** (for Nominal footprint).
  - Characteristics: A balanced middle ground between board density and manufacturing robustness. Average Pad size and Courtyard area.
  - Applications: The standard choice for most general-purpose commercial electronics. It provides stable solder attachments for typical reflow and wave soldering processes.
- **Density Level C: Minimum (Least) Land Protrusion**
  - IPC Designation: **L** (for Least footprint).
  - Characteristics: Uses the smallest Pad size and Courtyard area and courtyard area to achieve maximum component packing density.
  - Applications: Essential for space-constrained designs like mobile phones, handheld medical devices, and HDI (High-Density Interconnect) boards. Due to the small pads, rework is difficult.

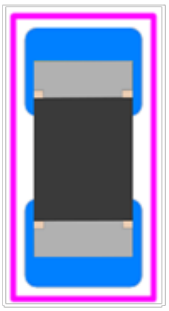
Select the correct level depending on your target manufacturing capability and the physical size constraints of your PCB. Using tools like the free PCB Libraries Footprint Expert Calculator or the Footprint Expert can help automatically generate these patterns based on component dimensions.



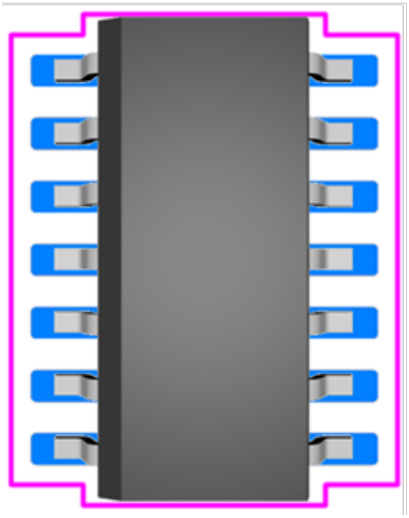
**Density Level A**
**Very Robust**
**Solder Joint**

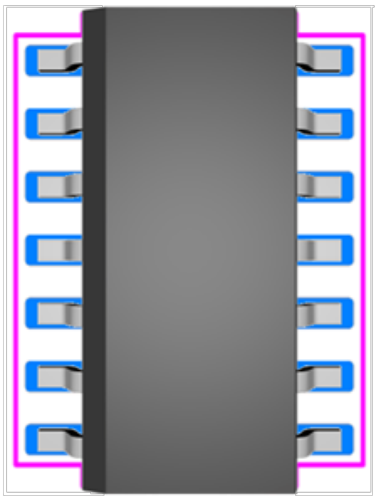


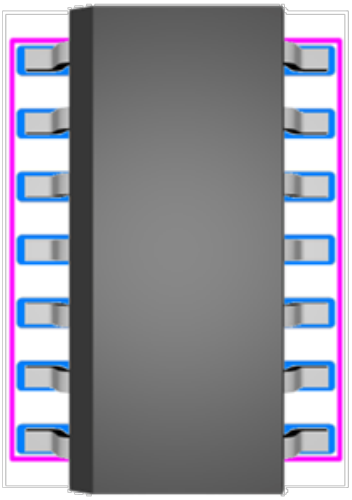
**Density Level B**
**General Purpose**
**Solder Joint**



**Density Level C**
**Minimum Solder Joint**
**High Density Applications**







## Summary of Differences

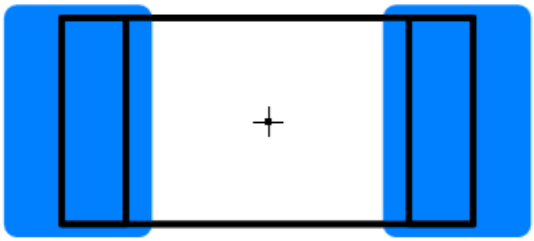
| Feature | Level A (Most) | Level B (Nominal) | Level C (Least) |
|---|---|---|---|
| **Pad Size** | Largest | Medium | Smallest |
| **Solder Fillet** | Maximum robust joint | Balanced | Minimal joint |
| **Ease of Rework** | Easy/Rework-friendly | Moderate | Very Difficult/None |
| **Main Usage** | High Reliability/Vibration | General Purpose | Micro-electronics (HDI) |
| **Acceptable Class** | 1,2,3 | 1,2,3 | 1,2 |

# 5.0 – IPC-7352 Mathematical Model

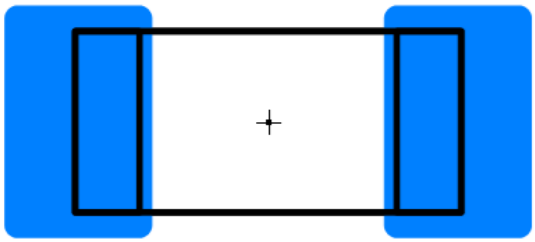
The IPC-7352 standard defines the mathematical model for creating reliable surface mount (SMD) PCB footprints by providing formulas to calculate pad width (X), pad spacing (G), and pad span (Z), based on component dimensions, solder fillet goals, and manufacturing tolerances.

The following images illustrate potential pad and terminal relationships under various Material Conditions – Minimum, Nominal, and Maximum.

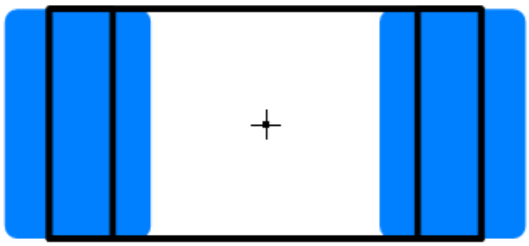
1. The Nominal Material condition of the component package & Nominal Terminal.



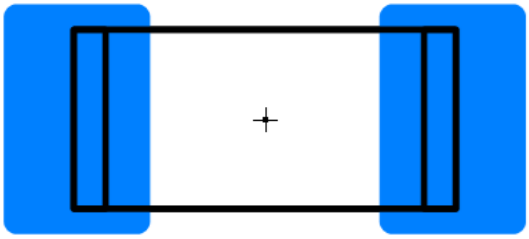
2. The Minimum Material condition of the component package & Nominal Terminal.



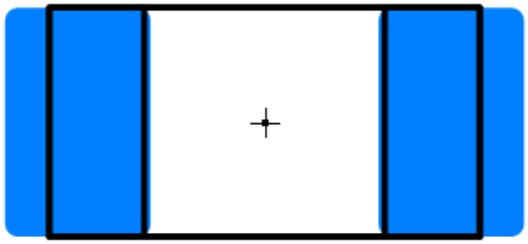
3. The Maximum Material condition of the component package & Nominal Terminal.



4. The Minimum Material condition of the component package & Minimum Terminal.



5. The Maximum Material condition of the component package & Maximum Terminal.

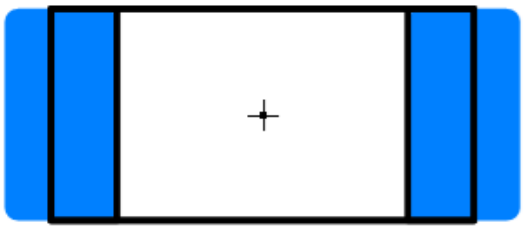


The resulting pad stack must have terminal leads on the pad stack regardless of every possible Material Condition possible to pass assembly inspection and meet the requirements set forth in the IPC J-STD-001 Standard and the IPC-7352 Guideline.

i.e.: regardless of the Component Package and Terminal Lead Material Condition, the Terminal Lead must never be exposed outside the calculated pad stack.

Note: most component packages are created in the Nominal Material Conditions. The package tolerances play a key role in the resulting pad stack.

6. Nominal Package Dimensions & no Package Tolerances.



**The Footprint Expert uses the IPC-7352 Mathematical Model.**
***For details, see IPC-7352*.**

# 6.0 – Surface Mount Solder Joint Goal Tables for Min/Max Calculation

The Min/Max Calculation section was originally inspired by **IPC-7351** and subsequently by the superseding **IPC-7352 – Generic Guideline for Land Pattern Design**. The solder joint goals were derived from the **IPC J-STD-001G - Requirements for Soldered Electrical and Electronic Assemblies**. For more details, see Appendix I.

### Gullwing Leads (SOP, QFP, SOT, DPAK, SOD)

| SOP / QFP | Least Density Level | | | | Nominal Density Level | | | | Most Density Level | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Terminal Lead Spacing | Toe | Heel | Side | Courtyard | Toe | Heel | Side | Courtyard | Toe | Heel | Side | Courtyard |
| Pitch > 1.00 mm | 0.30 | 0.40 | 0.05 | 0.10 | 0.35 | 0.45 | 0.06 | 0.20 | 0.40 | 0.50 | 0.07 | 0.40 |
| Pitch > 0.80, <= 1.00 mm | 0.25 | 0.35 | 0.04 | 0.10 | 0.30 | 0.40 | 0.05 | 0.20 | 0.35 | 0.45 | 0.06 | 0.40 |
| Pitch > 0.65, <= 0.80 mm | 0.20 | 0.30 | 0.03 | 0.10 | 0.25 | 0.35 | 0.04 | 0.20 | 0.30 | 0.40 | 0.05 | 0.40 |
| Pitch > 0.50, <= 0.65 mm | 0.15 | 0.25 | 0.01 | 0.10 | 0.20 | 0.30 | 0.02 | 0.20 | 0.25 | 0.35 | 0.03 | 0.40 |
| Pitch > 0.40, <= 0.50 mm | 0.10 | 0.20 | 0.00 | 0.10 | 0.15 | 0.25 | 0.00 | 0.20 | 0.20 | 0.30 | 0.00 | 0.40 |
| Pitch <= 0.40 mm | 0.10 | 0.20 | 0.00 | 0.10 | 0.15 | 0.25 | 0.00 | 0.20 | 0.20 | 0.30 | 0.00 | 0.40 |

| SOT | Least Density Level | | | | Nominal Density Level | | | | Most Density Level | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Terminal Lead Spacing | Toe | Heel | Side | Courtyard | Toe | Heel | Side | Courtyard | Toe | Heel | Side | Courtyard |
| Pitch > 1.92 mm | 0.20 | 0.30 | 0.05 | 0.10 | 0.25 | 0.35 | 0.06 | 0.20 | 0.30 | 0.40 | 0.07 | 0.40 |
| Pitch > 0.95, <= 1.92 mm | 0.15 | 0.20 | 0.04 | 0.10 | 0.20 | 0.25 | 0.05 | 0.20 | 0.25 | 0.30 | 0.06 | 0.40 |
| Pitch > 0.65, <= 0.95 mm | 0.15 | 0.20 | 0.03 | 0.10 | 0.20 | 0.25 | 0.04 | 0.20 | 0.25 | 0.30 | 0.05 | 0.40 |
| Pitch > 0.50, <= 0.65 mm | 0.10 | 0.15 | 0.01 | 0.10 | 0.15 | 0.20 | 0.02 | 0.20 | 0.20 | 0.25 | 0.03 | 0.40 |
| Pitch > 0.40, <= 0.50 mm | 0.10 | 0.15 | 0.00 | 0.10 | 0.15 | 0.20 | 0.00 | 0.20 | 0.20 | 0.25 | 0.00 | 0.40 |
| Pitch <= 0.40 mm | 0.10 | 0.15 | 0.00 | 0.10 | 0.15 | 0.20 | 0.00 | 0.20 | 0.20 | 0.25 | 0.00 | 0.40 |

| DPAK | Least Density Level | | | | Nominal Density Level | | | | Most Density Level | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Terminal Lead Spacing | Toe | Heel | Side | Courtyard | Toe | Heel | Side | Courtyard | Toe | Heel | Side | Courtyard |
| Pitch > 2.54 mm | 0.35 | 0.40 | 0.15 | 0.10 | 0.45 | 0.50 | 0.20 | 0.20 | 0.55 | 0.60 | 0.30 | 0.40 |
| Pitch > 2.28, <= 2.54 mm | 0.35 | 0.40 | 0.10 | 0.10 | 0.45 | 0.50 | 0.15 | 0.20 | 0.55 | 0.60 | 0.25 | 0.40 |
| Pitch > 1.70, <= 2.28 mm | 0.25 | 0.40 | 0.05 | 0.10 | 0.35 | 0.50 | 0.10 | 0.20 | 0.45 | 0.60 | 0.20 | 0.40 |
| Pitch > 1.27, <= 1.70 mm | 0.20 | 0.35 | 0.00 | 0.10 | 0.30 | 0.45 | 0.05 | 0.20 | 0.40 | 0.55 | 0.10 | 0.40 |
| Pitch <= 1.27 mm | 0.15 | 0.30 | 0.00 | 0.10 | 0.25 | 0.40 | 0.05 | 0.20 | 0.35 | 0.50 | 0.10 | 0.40 |

| SOD | Least Density Level | | | | Nominal Density Level | | | | Most Density Level | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Terminal Lead Spacing | Toe | Heel | Side | Courtyard | Toe | Heel | Side | Courtyard | Toe | Heel | Side | Courtyard |
| Pitch = None | 0.20 | 0.30 | 0.05 | 0.10 | 0.25 | 0.35 | 0.06 | 0.20 | 0.30 | 0.40 | 0.07 | 0.40 |

### Rectangular and Square-End Cap (Chips)

| Rectangular End Cap | Least Density Level | | | | Nominal Density Level | | | | Most Density Level | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Nominal Package Length | Toe | Heel | Side | Courtyard | Toe | Heel | Side | Courtyard | Toe | Heel | Side | Courtyard |
| Length > 4.75 mm | 0.40 | 0.00 | 0.00 | 0.10 | 0.50 | 0.00 | 0.00 | 0.20 | 0.60 | 0.00 | 0.05 | 0.40 |
| Length > 3.85, <= 4.75 mm | 0.30 | 0.00 | 0.00 | 0.10 | 0.40 | 0.00 | 0.00 | 0.20 | 0.50 | 0.00 | 0.05 | 0.40 |
| Length > 2.85, <= 3.85 mm | 0.25 | 0.00 | 0.00 | 0.10 | 0.35 | 0.00 | 0.00 | 0.20 | 0.45 | 0.00 | 0.05 | 0.40 |
| Length > 1.30, <= 2.85 mm | 0.20 | 0.00 | 0.00 | 0.10 | 0.30 | 0.00 | 0.00 | 0.20 | 0.40 | 0.00 | 0.05 | 0.40 |
| Length > 0.75, <= 1.30 mm | 0.15 | 0.00 | 0.00 | 0.10 | 0.20 | 0.00 | 0.00 | 0.15 | 0.25 | 0.00 | 0.00 | 0.20 |
| Length > 0.50, <= 0.75 mm | 0.08 | 0.00 | 0.00 | 0.10 | 0.10 | 0.00 | 0.00 | 0.15 | 0.12 | 0.00 | 0.00 | 0.20 |
| Length <= 0.50 mm | 0.04 | 0.00 | 0.00 | 0.10 | 0.05 | 0.00 | 0.00 | 0.15 | 0.06 | 0.00 | 0.00 | 0.20 |

## Inward L Lead Oscillator and Small Outline L-Lead (SOL)

| Inward L-Lead | Least Density Level | | | | Nominal Density Level | | | | Most Density Level | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Terminal Lead Spacing | Toe | Heel | Side | Courtyard | Toe | Heel | Side | Courtyard | Toe | Heel | Side | Courtyard |
| Pitch > 1.00 mm | 0.00 | 0.40 | 0.05 | 0.10 | 0.00 | 0.50 | 0.06 | 0.20 | 0.10 | 0.60 | 0.06 | 0.40 |
| Pitch > 0.80, <= 1.00 mm | 0.00 | 0.35 | 0.04 | 0.10 | 0.00 | 0.45 | 0.05 | 0.20 | 0.10 | 0.55 | 0.05 | 0.40 |
| Pitch > 0.65, <= 0.80 mm | 0.00 | 0.30 | 0.03 | 0.10 | 0.00 | 0.40 | 0.04 | 0.20 | 0.10 | 0.50 | 0.04 | 0.40 |
| Pitch > 0.50, <= 0.65 mm | 0.00 | 0.25 | 0.01 | 0.10 | 0.00 | 0.35 | 0.02 | 0.20 | 0.10 | 0.45 | 0.03 | 0.40 |
| Pitch > 0.40, <= 0.50 mm | 0.00 | 0.20 | 0.00 | 0.10 | 0.00 | 0.30 | 0.00 | 0.20 | 0.10 | 0.40 | 0.02 | 0.40 |
| Pitch <= 0.40 mm | 0.00 | 0.15 | 0.00 | 0.10 | 0.00 | 0.25 | 0.00 | 0.20 | 0.10 | 0.35 | 0.01 | 0.40 |

## Outward L-Lead (SOT)

| Outward L-Lead | Least Density Level | | | | Nominal Density Level | | | | Most Density Level | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Terminal Lead Spacing | Toe | Heel | Side | Courtyard | Toe | Heel | Side | Courtyard | Toe | Heel | Side | Courtyard |
| Pitch > 1.92 mm | 0.15 | 0.10 | 0.04 | 0.10 | 0.20 | 0.15 | 0.05 | 0.20 | 0.25 | 0.20 | 0.06 | 0.40 |
| Pitch > 0.95, <= 1.92 mm | 0.15 | 0.10 | 0.03 | 0.10 | 0.20 | 0.15 | 0.04 | 0.20 | 0.25 | 0.20 | 0.05 | 0.40 |
| Pitch > 0.65, <= 0.95 mm | 0.15 | 0.10 | 0.02 | 0.10 | 0.20 | 0.15 | 0.03 | 0.20 | 0.25 | 0.20 | 0.04 | 0.40 |
| Pitch > 0.50, <= 0.65 mm | 0.15 | 0.10 | 0.01 | 0.10 | 0.20 | 0.15 | 0.02 | 0.20 | 0.25 | 0.20 | 0.02 | 0.40 |
| Pitch > 0.40, <= 0.50 mm | 0.15 | 0.10 | 0.00 | 0.10 | 0.20 | 0.15 | 0.01 | 0.20 | 0.25 | 0.20 | 0.00 | 0.40 |
| Pitch <= 0.40 mm | 0.15 | 0.10 | 0.00 | 0.10 | 0.20 | 0.15 | 0.00 | 0.20 | 0.25 | 0.20 | 0.00 | 0.40 |

## Cylindrical End Cap (MELF)

| Cylindrical End Cap Nominal Diameter | Least Density Level | | | | Nominal Density Level | | | | Most Density Level | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Toe | Heel | Side | Courtyard | Toe | Heel | Side | Courtyard | Toe | Heel | Side | Courtyard |
| Dia. <= 1.00 | 0.10 | 0.00 | 0.05 | 0.10 | 0.30 | 0.05 | 0.15 | 0.20 | 0.50 | 0.10 | 0.25 | 0.40 |
| Dia. > 1.00 and <= 2.00 | 0.15 | 0.00 | 0.05 | 0.10 | 0.35 | 0.05 | 0.15 | 0.20 | 0.55 | 0.10 | 0.25 | 0.40 |
| Dia. > 2.00 and <= 3.00 | 0.20 | 0.00 | 0.05 | 0.10 | 0.40 | 0.05 | 0.15 | 0.20 | 0.60 | 0.10 | 0.25 | 0.40 |
| Dia. > 3.00 and <= 4.00 | 0.25 | 0.00 | 0.05 | 0.10 | 0.45 | 0.05 | 0.15 | 0.20 | 0.65 | 0.10 | 0.25 | 0.40 |
| Dia. > 4.00 | 0.30 | 0.00 | 0.05 | 0.10 | 0.50 | 0.05 | 0.15 | 0.20 | 0.70 | 0.10 | 0.25 | 0.40 |

## Small Outline No-Lead (SON, QFN)

| Flat No-lead Side | Least Density Level | | | | Nominal Density Level | | | | Most Density Level | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Toe | Heel | Side | Courtyard | Toe | Heel | Side | Courtyard | Toe | Heel | Side | Courtyard |
| SON and QFN | 0.10 | 0.00 | 0.00 | 0.10 | 0.20 | 0.00 | 0.00 | 0.20 | 0.30 | 0.00 | 0.00 | 0.40 |

## Small Outline Components, Flat Lead (SOFL, SODFL)

| Flat Lead | Least Density Level | | | | Nominal Density Level | | | | Most Density Level | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Toe | Heel | Side | Courtyard | Toe | Heel | Side | Courtyard | Toe | Heel | Side | Courtyard |
| SODFL and SOFL | 0.10 | 0.00 | 0.00 | 0.10 | 0.20 | 0.00 | 0.00 | 0.20 | 0.30 | 0.00 | 0.05 | 0.40 |

## Flat Lug Lead (DPAK)

| Flat Lug | Least Density Level | | | | Nominal Density Level | | | | Most Density Level | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Toe | Heel | Side | Courtyard | Toe | Heel | Side | Courtyard | Toe | Heel | Side | Courtyard |
| DPAK Tab | 0.20 | 0.00 | 0.00 | 0.10 | 0.35 | 0.03 | 0.03 | 0.20 | 0.50 | 0.06 | 0.06 | 0.40 |

## Small Outline Flat No-Lead Bottom (DFN, LGA, PSON, PQFN)

| Flat No-lead Bottom Only | Least Density Level | | Nominal Density Level | | Most Density Level | |
|---|---|---|---|---|---|---|
| Nominal Package Length | Periphery | Courtyard | Periphery | Courtyard | Periphery | Courtyard |
| Length >= 1.60 mm | 0.00 | 0.10 | 0.00 | 0.20 | 0.05 | 0.40 |
| Length < 1.60 mm | 0.00 | 0.10 | 0.00 | 0.15 | 0.00 | 0.20 |

## Under-Body Outward L-Lead (Aluminum Electrolytic Capacitor, Crystal)

| Under Body Outward L | Least Density Level | | | | Nominal Density Level | | | | Most Density Level | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Maximum Package Height | Toe | Heel | Side | Courtyard | Toe | Heel | Side | Courtyard | Toe | Heel | Side | Courtyard |
| Height > 10 mm | 0.40 | 0.00 | 0.40 | 0.20 | 0.70 | 0.00 | 0.50 | 0.40 | 1.00 | 0.10 | 0.60 | 0.80 |
| Height <= 10 mm | 0.30 | 0.00 | 0.30 | 0.10 | 0.50 | 0.00 | 0.40 | 0.20 | 0.70 | 0.05 | 0.50 | 0.40 |

## Inward Flat Ribbon L-Lead (Molded Body)

| Inward Flat Ribbon L-Lead | Least Density Level | | | | Nominal Density Level | | | | Most Density Level | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Maximum Package Height | Toe | Heel | Side | Courtyard | Toe | Heel | Side | Courtyard | Toe | Heel | Side | Courtyard |
| Height > 4.20 mm | 0.15 | 0.50 | 0.00 | 0.10 | 0.20 | 0.60 | 0.00 | 0.20 | 0.25 | 0.70 | 0.05 | 0.40 |
| Height > 3.20, <= 4.20 mm | 0.10 | 0.45 | 0.00 | 0.10 | 0.15 | 0.55 | 0.00 | 0.20 | 0.20 | 0.65 | 0.05 | 0.40 |
| Height > 2.20, <= 3.20 mm | 0.05 | 0.40 | 0.00 | 0.10 | 0.10 | 0.50 | 0.00 | 0.20 | 0.15 | 0.60 | 0.05 | 0.40 |
| Height > 1.20, <= 2.20 mm | 0.00 | 0.35 | 0.00 | 0.10 | 0.05 | 0.45 | 0.00 | 0.20 | 0.10 | 0.55 | 0.05 | 0.40 |
| Height <= 1.20 mm | 0.00 | 0.30 | 0.00 | 0.10 | 0.00 | 0.40 | 0.00 | 0.20 | 0.05 | 0.50 | 0.05 | 0.40 |

## Concave & Convex Chip Array and Leadless Chip Carrier (LCC)

| Side Lead | Least Density Level | | | | Nominal Density Level | | | | Most Density Level | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Terminal Lead Spacing | Toe | Heel | Side | Courtyard | Toe | Heel | Side | Courtyard | Toe | Heel | Side | Courtyard |
| Pitch > 2.54 mm | 0.45 | 0.02 | 0.00 | 0.10 | 0.55 | 0.04 | 0.00 | 0.20 | 0.65 | 0.06 | 0.01 | 0.40 |
| Pitch > 1.27, <= 2.54 mm | 0.40 | 0.00 | 0.00 | 0.10 | 0.50 | 0.02 | 0.00 | 0.20 | 0.60 | 0.04 | 0.00 | 0.40 |
| Pitch > 0.80, <= 1.27 mm | 0.35 | 0.00 | 0.00 | 0.10 | 0.45 | 0.00 | 0.00 | 0.20 | 0.55 | 0.02 | 0.00 | 0.40 |
| Pitch > 0.65, <= 0.80 mm | 0.25 | 0.00 | 0.00 | 0.10 | 0.35 | 0.00 | 0.00 | 0.20 | 0.45 | 0.00 | 0.00 | 0.40 |
| Pitch > 0.50, <= 0.65 mm | 0.20 | 0.00 | 0.00 | 0.10 | 0.30 | 0.00 | 0.00 | 0.20 | 0.40 | 0.00 | 0.00 | 0.40 |
| Pitch > 0.40, <= 0.50 mm | 0.15 | 0.00 | 0.00 | 0.10 | 0.25 | 0.00 | 0.00 | 0.20 | 0.35 | 0.00 | 0.00 | 0.40 |
| Pitch <= 0.40 mm | 0.10 | 0.00 | 0.00 | 0.10 | 0.20 | 0.00 | 0.00 | 0.20 | 0.30 | 0.00 | 0.00 | 0.40 |

| Side Lead | Least Density Level | | | | Nominal Density Level | | | | Most Density Level | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Lead Pitch | Toe | Heel | Side | Courtyard | Toe | Heel | Side | Courtyard | Toe | Heel | Side | Courtyard |
| Pitch = None | 0.25 | 0.00 | 0.00 | 0.10 | 0.35 | 0.00 | 0.00 | 0.20 | 0.45 | 0.00 | 0.00 | 0.40 |

## J-Leads

| J-Lead | Least Density Level | | | | Nominal Density Level | | | | Most Density Level | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Toe | Heel | Side | Courtyard | Toe | Heel | Side | Courtyard | Toe | Heel | Side | Courtyard |
| SOJ / OSC / PLCC | 0.00 | 0.15 | 0.01 | 0.10 | 0.00 | 0.35 | 0.03 | 0.20 | 0.10 | 0.55 | 0.05 | 0.40 |

## Column and Land Grid Array (CGA & LGA)

| Column and Land Grid Array (CGA & LGA) | | | | | | |
|---|---|---|---|---|---|---|
| Column Diameter | Adj. +/- % | Pad Variation | Pad Size Roundoff | Solder Mask Annular | Paste Mask Annular | Courtyard |
| 0.51 | 20% | 0.00 | 2 | 0.00 | 0.00 | 1.00 |

## Corner Concave Oscillator

| Corner Concave | Least Density Level | | | Nominal Density Level | | | Most Density Level | | |
|---|---|---|---|---|---|---|---|---|---|
| | Toe | Heel | Courtyard | Toe | Heel | Courtyard | Toe | Heel | Courtyard |
| Oscillator | 0.10 | 0.00 | 0.10 | 0.15 | 0.00 | 0.20 | 0.20 | 0.00 | 0.40 |

## Collapsing and Non-Collapsing Ball Grid Array (BGA)

| Collapsing Ball Grid Array (BGA) | | | | |
|---|---|---|---|---|
| Nominal Ball Diameter | Ball Size Reduction | Pad Variation | Pad Size Roundoff | Courtyard |
| 0.75 | 25% | 0.05 | 2 | 1.00 |
| 0.65 | 25% | 0.05 | 2 | 1.00 |
| 0.60 | 25% | 0.05 | 2 | 1.00 |
| 0.55 | 25% | 0.05 | 2 | 1.00 |
| 0.50 | 20% | 0.05 | 2 | 0.50 |
| 0.45 | 20% | 0.05 | 2 | 0.50 |
| 0.40 | 20% | 0.05 | 2 | 0.50 |
| 0.35 | 20% | 0.05 | 2 | 0.50 |
| 0.30 | 20% | 0.00 | 2 | 0.50 |
| 0.25 | 20% | 0.00 | 2 | 0.50 |
| 0.20 | 15% | 0.03 | 2 | 0.25 |
| 0.17 | 15% | 0.03 | 2 | 0.25 |
| 0.15 | 15% | 0.02 | 2 | 0.25 |

| Non-Collapsing Ball Grid Array (BGA) | | | | |
|---|---|---|---|---|
| Nominal Ball Diameter | Ball Size Increase | Pad Variation | Pad Size Roundoff | Courtyard |
| 0.75 | 15% | 0.05 | 2 | 1.00 |
| 0.65 | 15% | 0.05 | 2 | 1.00 |
| 0.60 | 15% | 0.05 | 2 | 1.00 |
| 0.55 | 15% | 0.05 | 2 | 1.00 |
| 0.50 | 10% | 0.05 | 2 | 0.50 |
| 0.45 | 10% | 0.05 | 2 | 0.50 |
| 0.40 | 10% | 0.05 | 2 | 0.50 |
| 0.35 | 10% | 0.05 | 2 | 0.50 |
| 0.30 | 10% | 0.05 | 2 | 0.50 |
| 0.25 | 10% | 0.05 | 2 | 0.50 |
| 0.20 | 5% | 0.03 | 2 | 0.25 |
| 0.17 | 5% | 0.03 | 2 | 0.25 |
| 0.15 | 5% | 0.03 | 2 | 0.25 |

# 7.0 – Solder Joint Goal Tables for Nominal Calculation

The Nominal Calculation section was inspired by the **FED Vol 18 – The New Proportional Land Dimensioning Concepts**. For more details, see Appendix I.

## Gullwing Leads (SOP, QFP, SOT, DPAK, SOD)

| SOP / QFP | Least Density Level | | | | Nominal Density Level | | | | Most Density Level | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Terminal Lead Spacing | Toe | Heel | Side | Courtyard | Toe | Heel | Side | Courtyard | Toe | Heel | Side | Courtyard |
| Pitch > 1.00 mm | 0.30 | 0.40 | 0.08 | 0.10 | 0.35 | 0.50 | 0.10 | 0.20 | 0.40 | 0.60 | 0.12 | 0.40 |
| Pitch > 0.80, <= 1.00 mm | 0.25 | 0.35 | 0.06 | 0.10 | 0.30 | 0.45 | 0.08 | 0.20 | 0.35 | 0.65 | 0.10 | 0.40 |
| Pitch > 0.65, <= 0.80 mm | 0.20 | 0.30 | 0.04 | 0.10 | 0.25 | 0.40 | 0.06 | 0.20 | 0.30 | 0.50 | 0.08 | 0.40 |
| Pitch > 0.50, <= 0.65 mm | 0.15 | 0.25 | 0.02 | 0.10 | 0.20 | 0.35 | 0.04 | 0.20 | 0.25 | 0.45 | 0.06 | 0.40 |
| Pitch > 0.40, <= 0.50 mm | 0.10 | 0.20 | 0.00 | 0.10 | 0.15 | 0.30 | 0.02 | 0.20 | 0.20 | 0.40 | 0.04 | 0.40 |
| Pitch <= 0.40 mm | 0.10 | 0.20 | 0.00 | 0.10 | 0.15 | 0.30 | 0.02 | 0.20 | 0.20 | 0.40 | 0.04 | 0.40 |

| SOT | Least Density Level | | | | Nominal Density Level | | | | Most Density Level | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Terminal Lead Spacing | Toe | Heel | Side | Courtyard | Toe | Heel | Side | Courtyard | Toe | Heel | Side | Courtyard |
| Pitch > 1.92 mm | 0.20 | 0.30 | 0.08 | 0.10 | 0.25 | 0.35 | 0.10 | 0.20 | 0.30 | 0.40 | 0.12 | 0.40 |
| Pitch > 0.95, <= 1.92 mm | 0.15 | 0.20 | 0.06 | 0.10 | 0.20 | 0.25 | 0.08 | 0.20 | 0.25 | 0.30 | 0.10 | 0.40 |
| Pitch > 0.65, <= 0.95 mm | 0.15 | 0.20 | 0.03 | 0.10 | 0.20 | 0.25 | 0.05 | 0.20 | 0.25 | 0.30 | 0.07 | 0.40 |
| Pitch > 0.50, <= 0.65 mm | 0.10 | 0.15 | 0.01 | 0.10 | 0.15 | 0.20 | 0.03 | 0.20 | 0.20 | 0.25 | 0.05 | 0.40 |
| Pitch > 0.40, <= 0.50 mm | 0.10 | 0.15 | 0.00 | 0.10 | 0.15 | 0.20 | 0.02 | 0.20 | 0.20 | 0.25 | 0.04 | 0.40 |
| Pitch <= 0.40 mm | 0.10 | 0.15 | 0.00 | 0.10 | 0.15 | 0.20 | 0.02 | 0.20 | 0.20 | 0.25 | 0.04 | 0.40 |

| DPAK | Least Density Level | | | | Nominal Density Level | | | | Most Density Level | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Terminal Lead Spacing | Toe | Heel | Side | Courtyard | Toe | Heel | Side | Courtyard | Toe | Heel | Side | Courtyard |
| Pitch > 2.54 mm | 0.35 | 0.50 | 0.20 | 0.10 | 0.45 | 0.60 | 0.25 | 0.20 | 0.55 | 0.70 | 0.30 | 0.40 |
| Pitch > 2.28, <= 2.54 mm | 0.35 | 0.50 | 0.15 | 0.10 | 0.45 | 0.60 | 0.20 | 0.20 | 0.55 | 0.70 | 0.25 | 0.40 |
| Pitch > 1.70, <= 2.28 mm | 0.25 | 0.50 | 0.10 | 0.10 | 0.35 | 0.60 | 0.15 | 0.20 | 0.45 | 0.70 | 0.20 | 0.40 |
| Pitch > 1.27, <= 1.70 mm | 0.20 | 0.45 | 0.05 | 0.10 | 0.30 | 0.55 | 0.10 | 0.20 | 0.40 | 0.65 | 0.15 | 0.40 |
| Pitch <= 1.27 mm | 0.15 | 0.40 | 0.05 | 0.10 | 0.25 | 0.50 | 0.10 | 0.20 | 0.35 | 0.60 | 0.15 | 0.40 |

| SOD | Least Density Level | | | | Nominal Density Level | | | | Most Density Level | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Terminal Lead Spacing | Toe | Heel | Side | Courtyard | Toe | Heel | Side | Courtyard | Toe | Heel | Side | Courtyard |
| Pitch = None | 0.15 | 0.20 | 0.05 | 0.10 | 0.20 | 0.30 | 0.10 | 0.20 | 0.25 | 0.40 | 0.15 | 0.40 |

## Rectangular and Square-End Cap (Chips)

| Rectangular End Cap | Least Density Level | | | | Nominal Density Level | | | | Most Density Level | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Nominal Package Length | Toe | Heel | Side | Courtyard | Toe | Heel | Side | Courtyard | Toe | Heel | Side | Courtyard |
| Length > 4.75 mm | 0.50 | 0.05 | 0.05 | 0.10 | 0.60 | 0.10 | 0.10 | 0.20 | 0.70 | 0.15 | 0.15 | 0.40 |
| Length > 3.85, <= 4.75 mm | 0.40 | 0.05 | 0.05 | 0.10 | 0.50 | 0.10 | 0.10 | 0.20 | 0.60 | 0.15 | 0.15 | 0.40 |
| Length > 2.85, <= 3.85 mm | 0.30 | 0.05 | 0.05 | 0.10 | 0.40 | 0.10 | 0.10 | 0.20 | 0.50 | 0.15 | 0.15 | 0.40 |
| Length > 1.30, <= 2.85 mm | 0.20 | 0.05 | 0.025 | 0.10 | 0.30 | 0.10 | 0.05 | 0.20 | 0.40 | 0.15 | 0.10 | 0.40 |
| Length > 0.75, <= 1.30 mm | 0.20 | 0.025 | 0.01 | 0.10 | 0.25 | 0.05 | 0.025 | 0.15 | 0.30 | 0.10 | 0.05 | 0.20 |
| Length > 0.50, <= 0.75 mm | 0.10 | 0.025 | 0.01 | 0.10 | 0.15 | 0.05 | 0.025 | 0.15 | 0.20 | 0.10 | 0.05 | 0.20 |
| Length <= 0.50 mm | 0.04 | 0.01 | 0.00 | 0.10 | 0.05 | 0.02 | 0.01 | 0.15 | 0.06 | 0.03 | 0.02 | 0.20 |

## Inward L Lead Oscillator and Small Outline L-Lead (SOL)

| Inward L-Lead | Least Density Level | | | | Nominal Density Level | | | | Most Density Level | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Terminal Lead Spacing | Toe | Heel | Side | Courtyard | Toe | Heel | Side | Courtyard | Toe | Heel | Side | Courtyard |
| Pitch > 1.00 mm | 0.05 | 0.40 | 0.06 | 0.10 | 0.10 | 0.50 | 0.08 | 0.20 | 0.15 | 0.60 | 0.10 | 0.40 |
| Pitch > 0.80, <= 1.00 mm | 0.05 | 0.40 | 0.05 | 0.10 | 0.10 | 0.50 | 0.07 | 0.20 | 0.15 | 0.60 | 0.09 | 0.40 |
| Pitch > 0.65, <= 0.80 mm | 0.05 | 0.35 | 0.04 | 0.10 | 0.10 | 0.45 | 0.06 | 0.20 | 0.15 | 0.55 | 0.08 | 0.40 |
| Pitch > 0.50, <= 0.65 mm | 0.05 | 0.30 | 0.03 | 0.10 | 0.10 | 0.40 | 0.05 | 0.20 | 0.15 | 0.50 | 0.07 | 0.40 |
| Pitch > 0.40, <= 0.50 mm | 0.05 | 0.25 | 0.02 | 0.10 | 0.10 | 0.35 | 0.04 | 0.20 | 0.15 | 0.45 | 0.06 | 0.40 |
| Pitch <= 0.40 mm | 0.05 | 0.20 | 0.01 | 0.10 | 0.10 | 0.30 | 0.03 | 0.20 | 0.15 | 0.40 | 0.05 | 0.40 |

## Outward L-Lead (SOT)

| Outward L-Lead | Least Density Level | | | | Nominal Density Level | | | | Most Density Level | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Terminal Lead Spacing | Toe | Heel | Side | Courtyard | Toe | Heel | Side | Courtyard | Toe | Heel | Side | Courtyard |
| Pitch > 1.92 mm | 0.15 | 0.10 | 0.08 | 0.10 | 0.20 | 0.15 | 0.10 | 0.20 | 0.25 | 0.20 | 0.12 | 0.40 |
| Pitch > 0.95, <= 1.92 mm | 0.15 | 0.10 | 0.06 | 0.10 | 0.20 | 0.15 | 0.08 | 0.20 | 0.25 | 0.20 | 0.10 | 0.40 |
| Pitch > 0.65, <= 0.95 mm | 0.15 | 0.10 | 0.03 | 0.10 | 0.20 | 0.15 | 0.05 | 0.20 | 0.25 | 0.20 | 0.04 | 0.40 |
| Pitch > 0.50, <= 0.65 mm | 0.15 | 0.10 | 0.01 | 0.10 | 0.20 | 0.15 | 0.03 | 0.20 | 0.25 | 0.20 | 0.02 | 0.40 |
| Pitch > 0.40, <= 0.50 mm | 0.15 | 0.10 | 0.00 | 0.10 | 0.20 | 0.15 | 0.02 | 0.20 | 0.25 | 0.20 | 0.00 | 0.40 |
| Pitch <= 0.40 mm | 0.15 | 0.10 | 0.00 | 0.10 | 0.20 | 0.15 | 0.02 | 0.20 | 0.25 | 0.20 | 0.00 | 0.40 |

## Cylindrical End Cap (MELF)

| Cylindrical End Cap Nominal Diameter | Least Density Level | | | | Nominal Density Level | | | | Most Density Level | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Toe | Heel | Side | Courtyard | Toe | Heel | Side | Courtyard | Toe | Heel | Side | Courtyard |
| Dia. <= 1.00 | 0.15 | 0.05 | 0.10 | 0.10 | 0.35 | 0.10 | 0.20 | 0.20 | 0.55 | 0.15 | 0.30 | 0.40 |
| Dia. > 1.00 and <= 2.00 | 0.20 | 0.05 | 0.10 | 0.10 | 0.40 | 0.10 | 0.20 | 0.20 | 0.60 | 0.15 | 0.30 | 0.40 |
| Dia. > 2.00 and <= 3.00 | 0.25 | 0.05 | 0.10 | 0.10 | 0.45 | 0.10 | 0.20 | 0.20 | 0.65 | 0.15 | 0.30 | 0.40 |
| Dia. > 3.00 and <= 4.00 | 0.30 | 0.05 | 0.10 | 0.10 | 0.50 | 0.10 | 0.20 | 0.20 | 0.70 | 0.15 | 0.30 | 0.40 |
| Dia. > 4.00 | 0.30 | 0.05 | 0.10 | 0.10 | 0.50 | 0.10 | 0.20 | 0.20 | 0.70 | 0.15 | 0.30 | 0.40 |

## Small Outline No-Lead (SON, QFN)

| Flat No-lead Side | Least Density Level | | | | Nominal Density Level | | | | Most Density Level | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Toe | Heel | Side | Courtyard | Toe | Heel | Side | Courtyard | Toe | Heel | Side | Courtyard |
| SON and QFN | 0.15 | 0.00 | 0.00 | 0.10 | 0.25 | 0.05 | 0.025 | 0.20 | 0.35 | 0.10 | 0.05 | 0.40 |

## Small Outline Components, Flat Lead (SOFL, SODFL)

| Flat Lead | Least Density Level | | | | Nominal Density Level | | | | Most Density Level | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Toe | Heel | Side | Courtyard | Toe | Heel | Side | Courtyard | Toe | Heel | Side | Courtyard |
| SODFL and SOFL | 0.15 | 0.00 | 0.00 | 0.10 | 0.25 | 0.05 | 0.025 | 0.15 | 0.35 | 0.10 | 0.05 | 0.20 |

## Flat Lug Lead (DPAK)

| Flat Lug | Least Density Level | | | | Nominal Density Level | | | | Most Density Level | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Toe | Heel | Side | Courtyard | Toe | Heel | Side | Courtyard | Toe | Heel | Side | Courtyard |
| DPAK Tab | 0.25 | 0.02 | 0.02 | 0.10 | 0.40 | 0.05 | 0.05 | 0.20 | 0.55 | 0.08 | 0.08 | 0.40 |

## Small Outline Flat No-Lead Bottom (DFN, PSON, PQFN)

| Flat No-lead Bottom Only | Least Density Level | | Nominal Density Level | | Most Density Level | |
|---|---|---|---|---|---|---|
| Nominal Package Length | Periphery | Courtyard | Periphery | Courtyard | Periphery | Courtyard |
| Length >= 1.60 mm | 0.025 | 0.10 | 0.05 | 0.20 | 0.10 | 0.40 |
| Length < 1.60 mm | 0.00 | 0.10 | 0.025 | 0.15 | 0.05 | 0.20 |

## Under-Body Outward L-Lead (Aluminum Electrolytic Capacitor, Crystal)

| Under Body Outward L | Least Density Level | | | | Nominal Density Level | | | | Most Density Level | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Maximum Package Height | Toe | Heel | Side | Courtyard | Toe | Heel | Side | Courtyard | Toe | Heel | Side | Courtyard |
| Height > 10 mm | 0.60 | 0.10 | 0.50 | 0.20 | 0.80 | 0.15 | 0.60 | 0.40 | 1.00 | 0.20 | 0.70 | 0.80 |
| Height <= 10 mm | 0.40 | 0.05 | 0.40 | 0.10 | 0.60 | 0.10 | 0.50 | 0.20 | 0.80 | 0.15 | 0.60 | 0.40 |

## Inward Flat Ribbon L-Lead (Molded Body)

| Inward Flat Ribbon L-Lead | Least Density Level | | | | Nominal Density Level | | | | Most Density Level | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Maximum Package Height | Toe | Heel | Side | Courtyard | Toe | Heel | Side | Courtyard | Toe | Heel | Side | Courtyard |
| Height > 4.20 mm | 0.20 | 0.55 | 0.00 | 0.10 | 0.25 | 0.65 | 0.05 | 0.20 | 0.30 | 0.75 | 0.10 | 0.40 |
| Height > 3.20, <= 4.20 mm | 0.20 | 0.55 | 0.00 | 0.10 | 0.25 | 0.65 | 0.05 | 0.20 | 0.30 | 0.75 | 0.10 | 0.40 |
| Height > 2.20, <= 3.20 mm | 0.15 | 0.50 | 0.00 | 0.10 | 0.20 | 0.60 | 0.05 | 0.20 | 0.25 | 0.70 | 0.10 | 0.40 |
| Height > 1.20, <= 2.20 mm | 0.10 | 0.45 | 0.00 | 0.10 | 0.15 | 0.55 | 0.05 | 0.20 | 0.20 | 0.65 | 0.10 | 0.40 |
| Height <= 1.20 mm | 0.05 | 0.40 | 0.00 | 0.10 | 0.10 | 0.50 | 0.05 | 0.20 | 0.15 | 0.60 | 0.10 | 0.40 |

## Concave & Convex Chip Array and Leadless Chip Carrier (LCC)

| Side Lead | Least Density Level | | | | Nominal Density Level | | | | Most Density Level | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Terminal Lead Spacing | Toe | Heel | Side | Courtyard | Toe | Heel | Side | Courtyard | Toe | Heel | Side | Courtyard |
| Pitch > 2.54 mm | 0.45 | 0.10 | 0.08 | 0.10 | 0.55 | 0.12 | 0.10 | 0.20 | 0.65 | 0.14 | 0.12 | 0.40 |
| Pitch > 1.27, <= 2.54 mm | 0.40 | 0.08 | 0.05 | 0.10 | 0.50 | 0.10 | 0.07 | 0.20 | 0.60 | 0.12 | 0.09 | 0.40 |
| Pitch > 0.80, <= 1.27 mm | 0.35 | 0.06 | 0.03 | 0.10 | 0.45 | 0.08 | 0.05 | 0.20 | 0.55 | 0.10 | 0.07 | 0.40 |
| Pitch > 0.65, <= 0.80 mm | 0.25 | 0.04 | 0.01 | 0.10 | 0.35 | 0.06 | 0.03 | 0.20 | 0.45 | 0.08 | 0.05 | 0.40 |
| Pitch > 0.50, <= 0.65 mm | 0.20 | 0.02 | 0.00 | 0.10 | 0.30 | 0.04 | 0.01 | 0.20 | 0.40 | 0.06 | 0.03 | 0.40 |
| Pitch > 0.40, <= 0.50 mm | 0.15 | 0.00 | 0.00 | 0.10 | 0.25 | 0.02 | 0.00 | 0.20 | 0.35 | 0.04 | 0.01 | 0.40 |
| Pitch <= 0.40 mm | 0.10 | 0.00 | 0.00 | 0.10 | 0.20 | 0.02 | 0.00 | 0.20 | 0.30 | 0.04 | 0.01 | 0.40 |

| Side Lead | Least Density Level | | | | Nominal Density Level | | | | Most Density Level | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Lead Pitch | Toe | Heel | Side | Courtyard | Toe | Heel | Side | Courtyard | Toe | Heel | Side | Courtyard |
| Pitch = None | 0.25 | 0.00 | 0.00 | 0.10 | 0.35 | 0.05 | 0.05 | 0.20 | 0.45 | 0.10 | 0.10 | 0.40 |

## J-Leads

| J-Lead | Least Density Level | | | | Nominal Density Level | | | | Most Density Level | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Toe | Heel | Side | Courtyard | Toe | Heel | Side | Courtyard | Toe | Heel | Side | Courtyard |
| SOJ / OSC / PLCC | 0.05 | 0.20 | 0.04 | 0.10 | 0.10 | 0.40 | 0.07 | 0.20 | 0.15 | 0.60 | 0.10 | 0.40 |

## Column and Land Grid Array (CGA & LGA)

| Column and Land Grid Array (CGA & LGA) | | | | | | |
|---|---|---|---|---|---|---|
| Column Diameter | Adj. +/- % | Pad Variation | Pad Size Roundoff | Solder Mask Annular | Paste Mask Annular | Courtyard |
| 0.51 | 20% | 0.00 | 2 | 0.00 | 0.00 | 1.00 |

## Corner Concave Oscillator

| Corner Concave | Least Density Level | | | Nominal Density Level | | | Most Density Level | | |
|---|---|---|---|---|---|---|---|---|---|
| | Toe | Heel | Courtyard | Toe | Heel | Courtyard | Toe | Heel | Courtyard |
| Oscillator | 0.10 | 0.00 | 0.10 | 0.20 | 0.05 | 0.20 | 0.30 | 0.10 | 0.40 |

## Collapsing and Non-Collapsing Ball Grid Array (BGA)

| Collapsing Ball Grid Array (BGA) | | | | |
|---|---|---|---|---|
| Nominal Ball Diameter | Ball Size Reduction | Pad Variation | Pad Size Roundoff | Courtyard |
| 0.75 | 25% | 0.05 | 2 | 1.00 |
| 0.65 | 25% | 0.05 | 2 | 1.00 |
| 0.60 | 25% | 0.05 | 2 | 1.00 |
| 0.55 | 25% | 0.05 | 2 | 1.00 |
| 0.50 | 20% | 0.05 | 2 | 0.50 |
| 0.45 | 20% | 0.05 | 2 | 0.50 |
| 0.40 | 20% | 0.05 | 2 | 0.50 |
| 0.35 | 20% | 0.05 | 2 | 0.50 |
| 0.30 | 20% | 0.00 | 2 | 0.50 |
| 0.25 | 20% | 0.00 | 2 | 0.50 |
| 0.20 | 15% | 0.03 | 2 | 0.25 |
| 0.17 | 15% | 0.03 | 2 | 0.25 |
| 0.15 | 15% | 0.02 | 2 | 0.25 |

| Non-Collapsing Ball Grid Array (BGA) | | | | |
|---|---|---|---|---|
| Nominal Ball Diameter | Ball Size Increase | Pad Variation | Pad Size Roundoff | Courtyard |
| 0.75 | 15% | 0.05 | 2 | 1.00 |
| 0.65 | 15% | 0.05 | 2 | 1.00 |
| 0.60 | 15% | 0.05 | 2 | 1.00 |
| 0.55 | 15% | 0.05 | 2 | 1.00 |
| 0.50 | 10% | 0.05 | 2 | 0.50 |
| 0.45 | 10% | 0.05 | 2 | 0.50 |
| 0.40 | 10% | 0.05 | 2 | 0.50 |
| 0.35 | 10% | 0.05 | 2 | 0.50 |
| 0.30 | 10% | 0.05 | 2 | 0.50 |
| 0.25 | 10% | 0.05 | 2 | 0.50 |
| 0.20 | 5% | 0.03 | 2 | 0.25 |
| 0.17 | 5% | 0.03 | 2 | 0.25 |
| 0.15 | 5% | 0.03 | 2 | 0.25 |

# 8.0 – Manufacturer Recommended Patterns

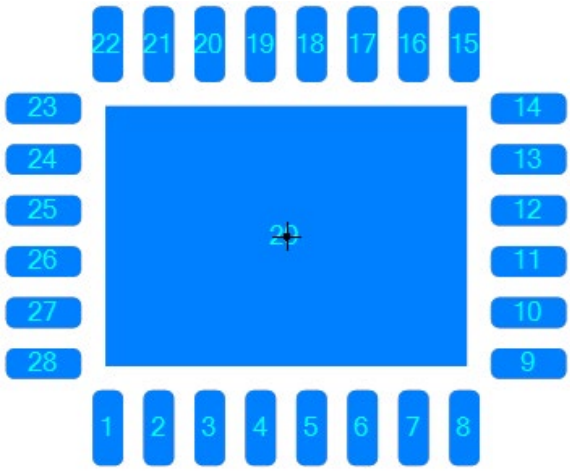
All non-standard packages must use the recommended manufacturer pattern.

The misconception that simply using the manufacturer recommended pattern will keep you safe is enough to get you in serious trouble, and over time, create mayhem in your CAD library. You need much more than the recommended pattern for a reliable PCB design!

Most component manufacturers provide recommended solder patterns in their datasheets, but there are two major issues you need to consider:

1. What rules were used to calculate the mfr. recommended solder pattern, and are they consistent across your library of parts for different manufacturers?
2. Since manufacturers provide no drafting outline data, how are you consistently creating these and applying them throughout your library over time?
3. Did the component manufacturer create reference PC boards and run them through stress tests to check their solder joint goals against the IPC J-STD-001 standard?
4. Component manufacturer recommended patterns are typically designed using nominal package dimensions; does the recommended pattern also accommodate the minimum and maximum material condition of the package tolerances specified in their datasheet?

Here is a representation of a Manufacturer Recommended Pattern with rounded rectangle pad shape. All component manufacturers (except Texas Instruments) recommended rectangle pad shape. However, paste mask stencil apertures are laser cut with rounded corners.



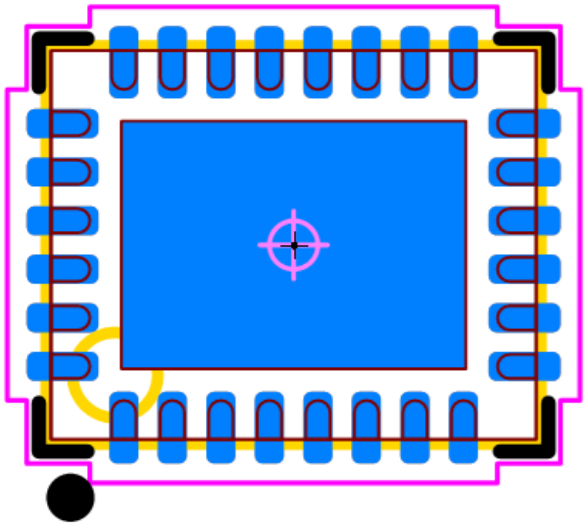

This is obviously missing the six critical drafting outlines. Traditionally, these have been manually created with a plethora of inconsistent rules that get adjusted over time:

1. Silkscreen
2. Assembly
3. Courtyard
4. Origin
5. Component
6. Terminals

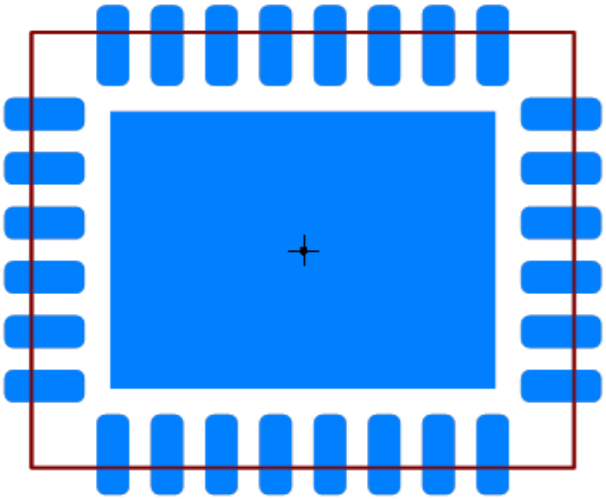
It takes more time to manually add all the necessary Drafting Outlines than it does to create the Manufacturer Recommended Pattern, and these are just as important as the pattern itself!

All drafting outline widths and spacings are defined in your personal master Options file. This guarantees consistent quality throughout your entire CAD library. You can also turn off any drafting outline that you do not want in your CAD library, but easily “bring it back” if you decide later that you need it!

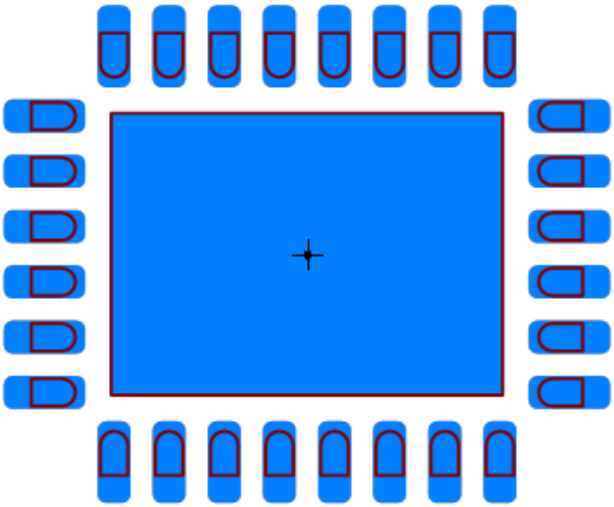
This is your end goal, read on for details how to reach it:



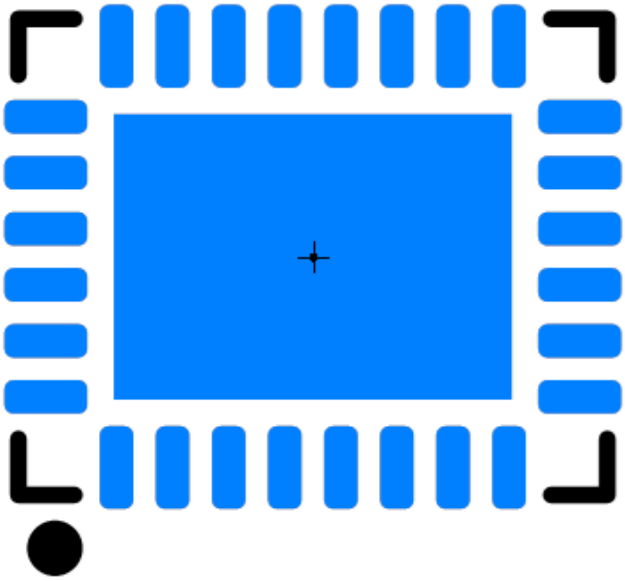
The Component Outline is crucial for accurate assembly placement and helps ensure your components fit properly on the board. It helps with verification during visual inspections, and facilitates repair, rework, and future updates to the design.



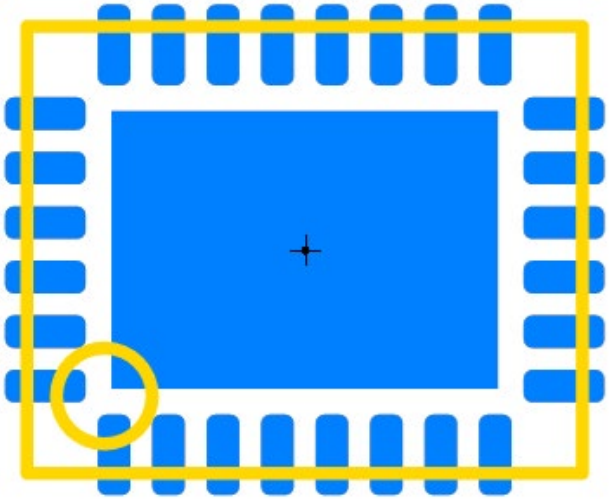
The Terminal Outlines are likewise critically important. They represent where on the metal terminal leads the physical package makes contact to the PCB. These are essential for reliable soldering and proper electrical connectivity. Each terminal lead outline must be entirely located on a pad. If the pad is not 100% on a metalized terminal outline, then the manufacturer's recommended pattern is not good, and you will get a bad solder connection.



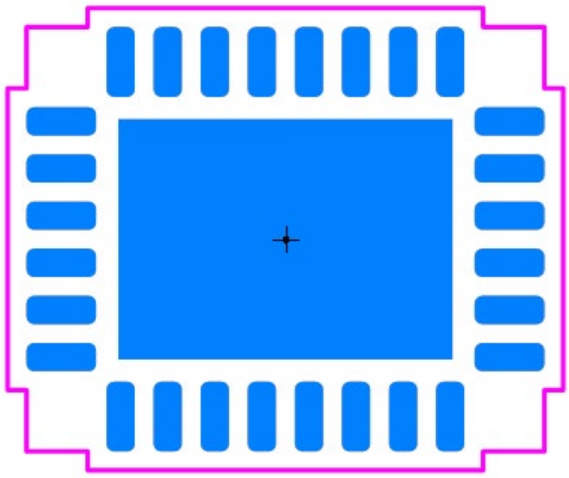
The Silkscreen Outline enables proper component orientation and should be created so that it's visible after assembly. Silkscreen outlines should not be placed under the package body – they are useless there and could potentially lift low profile or micro-miniature components off the PCB surface resulting in poor solder joints. The silkscreen data includes a post assembly inspection dot located by Pin 1, which helps with final assembly inspection.



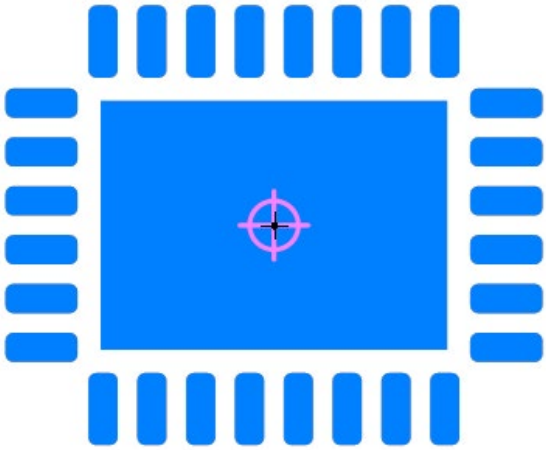
The Assembly Outline is a closed polygon. A chamfered corner is located by Pin 1 if the component is polarized or cannot be inverted during assembly. The assembly outline is important because it provides clear reference points for automated pick-and-place machines. A well-defined Assembly Outline also facilitates design verification and quality control.



The Courtyard Outline is extremely important in defining the required minimum clearance area required for a component, ensuring there is no interference with neighboring components during assembly or operation. The ideal shape is contoured around the package body and pads, which is the default setting in the Footprint Expert. The courtyard excess value for Package Body and Pads can be set separately.



The Origin Outlines are placed on an independent layer. The size & outline width are user definable. Accuracy is essential for accurate alignment because it serves as a reference for positioning the component on the PCB. A precise origin simplifies machine programming and enhances design portability across tools.



Datasheet dimensional tolerances are usually a conservative envelope rather than the real production distribution. If/when measurement data shows the parts are tightly controlled – Six Sigma quality levels – designing footprint geometry using nominal dimensions instead of worst-case maximum material condition can give us a reliable solder joint and provide space for routing. Having real measurement distribution data could support a change toward using nominal measurements.

For standard components, we can round the corners of any rectangular pads with a ~0.05 mm corner radius. This eases routing with little to no reliability trade-off, and on tight-pitch QFNs it buys extra corner clearance, which reduces the chance of solder mask slivers. If the manufacturer's QFN pads are a D-shape/finger shape with a full round on the heel side nearest the EPAD, match that shape for the same reason – there is very little downside, and it helps corner clearance.

Footprint Expert can output the terminal outlines and show where the physical part lands on the pads. Adding a 3D model to visually confirm footprint-to-component compatibility is also very helpful – Footprint Expert generates both the footprint and the 3D model for standard packages on the same origin and orientation. For non-standard parts, finding the most detailed manufacturer model available and stacking it against the pattern in CAD is another check I'd recommend.

A few package types genuinely benefit from following the manufacturer's recommendation.

*Example:* Texas Instruments (TI) provides highly detailed recommended patterns for every Case Code they develop. Their pad stack patterns are almost predicable because they use the same terminal lead width and length for each pin pitch for each component family. TI provides solder mask data that always has a solder mask web between the pads. It's as if they created their terminal lead widths intentionally to avoid gang masking rows of pins. The paste mask apertures for thermal pads always have a 0.20 mm aperture gap, a 0.05 mm corner radius on every aperture and they provide 80% paste mask coverage. They recommend a 0.05 mm corner radius on every pad stack while most component manufacturers recommend a rectangular pad shape and no solder or paste mask recommendations. TI is one of the most organized component manufacturers with consistent quality. Their Case Code packages are used by multiple part numbers, and many TI Case Codes are assigned to thousands of part numbers.

**Thermal-Pad Paste Mask:** Manufacturers typically recommend a paste pattern other than 1:1 with the metallized area, because excessive paste floats and rotates the part during reflow, risking pin-to-pin shorting and open perimeter joints. IPC-7093 covers the windowpane/array aperture with coverage commonly in the ~50–80% range. Footprint Expert hits the coverage target through the options file, which saves hand-drawing each paste block.

**Tight-tolerance Guide Pins or Press-Fit Pins:** Go with the manufacturer's recommendation. Guide pins and press-fit finished-hole size and tolerance are manufacturer-specific (compliant-pin design) and should come straight from their drawing.

**High-Power Pads:** The recommended pad may be larger than the calculated one to add heat dissipation and reduce thermal-cycling fatigue. Here we can solder mask-define the pad: the copper layer uses the manufacturer's larger recommended size for heat spreading and mechanical robustness, and the solder mask opening uses the Footprint Expert-calculated land, since the mask edge is what defines the solderable area.

**High-Voltage Applications:** The recommended pads may be spaced further apart than the Footprint Expert lands. Use IPC-2221B to confirm the pattern is acceptable for the given voltage.

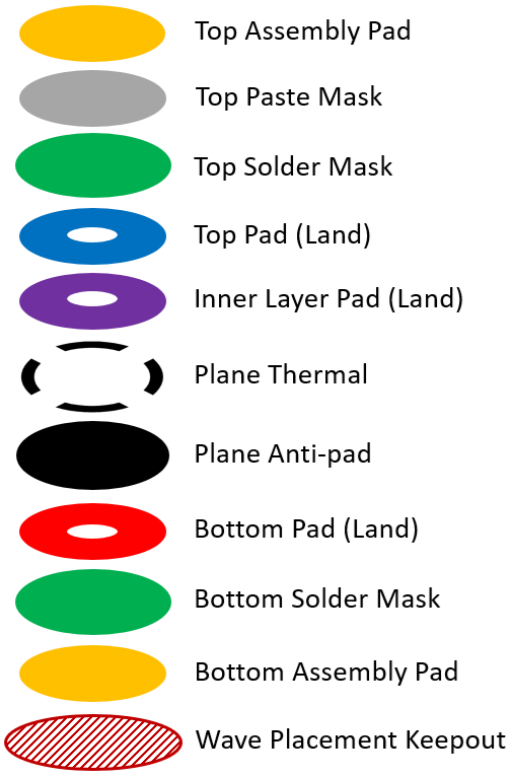
**RF Components:** Follow the manufacturer's recommendation as closely as possible. These almost always ship with an evaluation board demonstrating tested performance across the listed parameter range, which is a reliable starting point. RF engineers typically begin from that recommendation and modify based on bench data or EM simulation for their specific needs.

**Die Components:** Also, a case to follow the manufacturer closely – though these often have no recommendation. Working with die means an advanced process/fab house by definition, so we can build the pad stack 1:1 with the die-bump metallization with no solder mask expansion, use the CAD tool's layer capabilities to assign double-sided features that must count electrically in the schematic, and define plated or non-plated contours for cavity-mounted applications.

# 9.0 – Through-hole Terminals

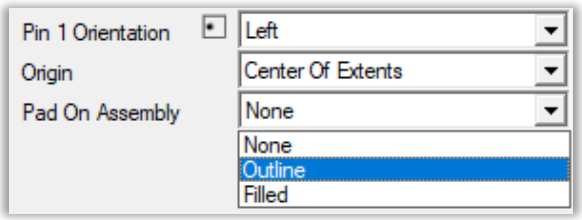
A **through-hole pad stack** is a set of Printed Circuit Board features that define a plated or non-plated, drilled hole that: 1. accommodates a component terminal lead; 2. Provides or prevents a connective path between layered circuitry; or both.

**Elements of a Through-hole Pad Stack**




**Pad on Assembly Layer**

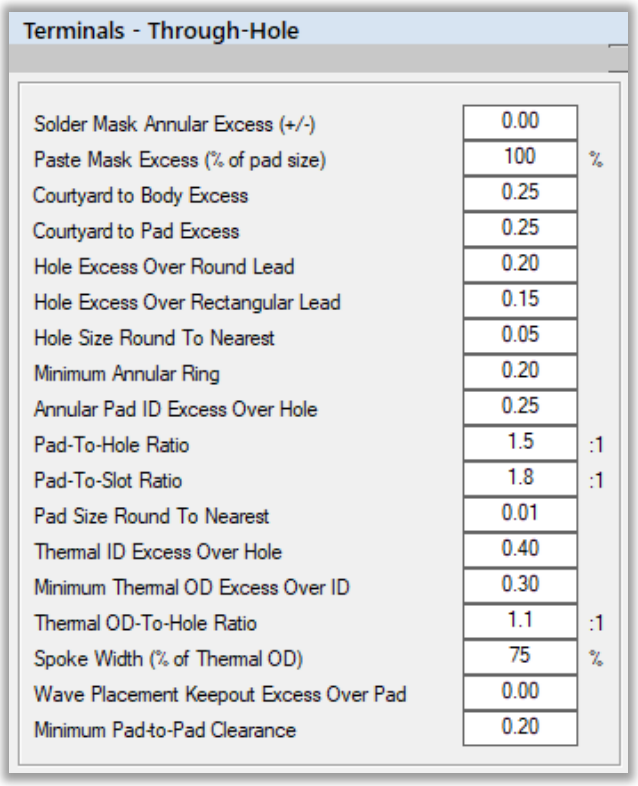
This is a unique, user selectable pad stack option in that it is defined as a ***Component*** option.




When ***Outline*** is selected, graphics, created from the Top and Bottom pads, are added as drawing line elements on the respective footprint Assembly Layers.

When ***Filled*** is selected, regular filled pads are added to the terminal pad stack on the Top and Bottom Assembly layers.

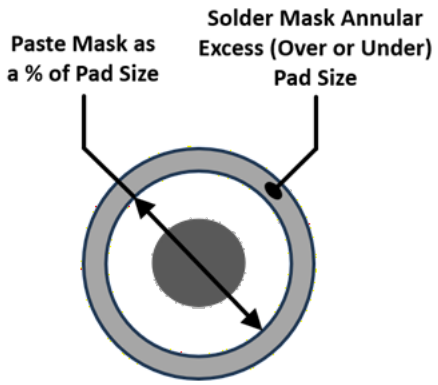
**Footprint Expert Options for Through-hole Pad Stacks**




**Solder and Paste Mask Excess**

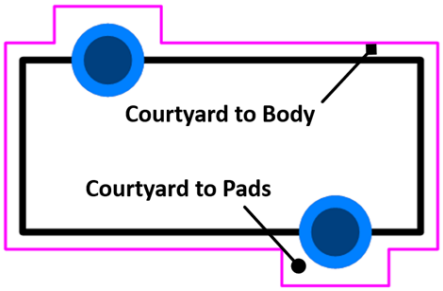
The **Solder Mask Excess** option sets the size of the solder mask pad relative to the top or bottom pads, respectively. The value is expressed as either over (pad plus excess) or under (pad minus excess).

**Paste Mask**, when applied to through-hole pad stacks and referred to as "**Pin-in-Paste**", is an advanced soldering technique that integrates through-hole and surface mount components in a single reflow pass. This method involves depositing solder paste inside through-hole vias and pads before component placement, allowing for soldering through-hole pins and the PCB in one step. Paste mask size is typically smaller than their associated and expressed as percentage of its associated pad size.



**Courtyard Clearance to Pad and Body**

While these values appear as pad stack options, they don't appear anywhere as physical features in the pad stack itself. Their effect is only noticeable in the courtyard outline spacing surrounding the footprint. A value of zero applied to either option results in a courtyard with no clearance to that option.

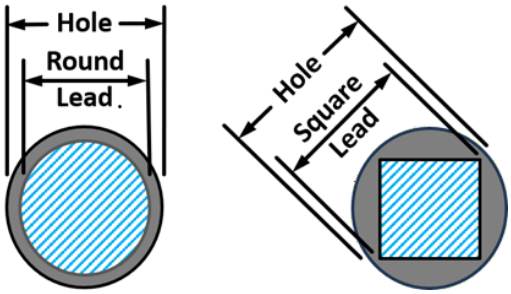



**Hole Excess over Lead**

There are two possible value choices for this option. Hole **Excess to Round** or **Excess to Square/Rectangular** leads.

The excess value sets a round hole diameter equal to the round lead diameter or the square/rectangular lead diagonal, plus the specified hole over lead clearance.

Example: square lead = 0.50; lead diagonal = 0.707; hole over lead = 0.15; hole diameter = 0.707 + 0.15 = 0.857.

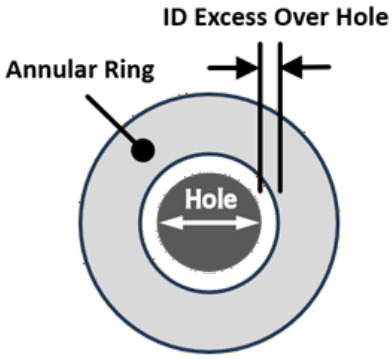



**Hole Size Round To Nearest**

This option is applied the result of the hole calculation to force a finished hole value to be rounded up so as to be evenly divisible by this value. Setting this value to zero will allow a hole size to round off to the Design Options units decimal place setting.
Example: round 0.857 up to the nearest 0.05 = 0.90.

**Annular Ring**

The **Annular Ring** is a pad with an inner diameter that maintains a clearance to a plated or non-plated hole. It is defined by two values: a pad outer diameter (or length and width) and a uniform excess spacing of the inner pad dimensions to the hole perimeter.

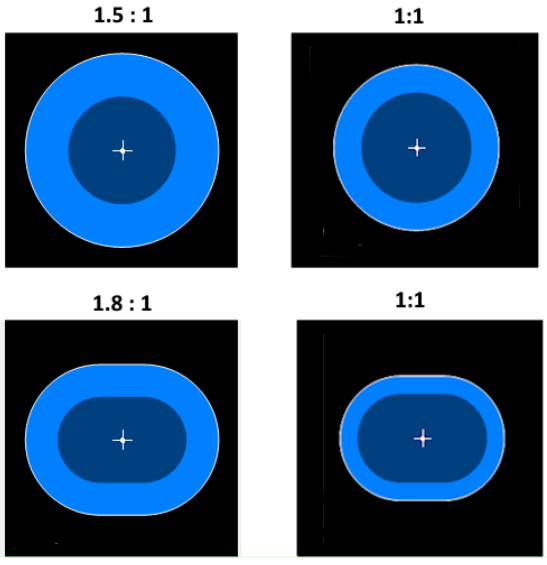



**Pad-To-Hole and Slot Ratios**

Optional ratios can be applied to pad stack calculations that provide an additional robustness that grows in proportion to the hole or slot size.

In practice, the pad size is initially derived as ratio to the hole size then other settings (such as Minimum Annular Ring, etc.) can be applied as required.

The effect of ratios on pad size is illustrated below. Hole and slot sizes shown are equal and all other through-hole option settings are the same.



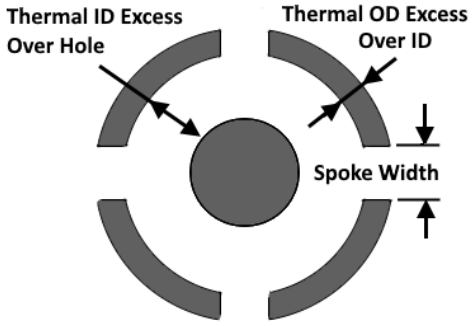

Example (round hole and pad):
Hole = 0.70; Pad = Hole x Ratio = 0.70 x 1.5 = 1.05.

**Pad Size Round-To-Nearest**
This option is applied to the result of the pad calculation to force a finished pad value to be rounded off so as to be evenly divisible by this value. Setting this value to zero will allow a pad size to round off to the Design Options units decimal place setting.

Example: round 1.05 up to the nearest 0.1 = 1.10.

**Thermal Relief**
A Thermal relief, also called a thermal pad, is a pattern of copper strips, or 'spokes' connecting a PCB pad, across a void, to a large copper area, such as a ground or power plane. Unlike a solid connection, a thermal relief limits heat transfer, preventing the copper plane from acting as a heat sink that could result in a 'cold' solder joint.

**Thermal Relief Options**




**Thermal ID Excess Over Hole**
Defines the conductive clad space between the hole and the thermal void inner diameter.

**Thermal OD Excess Over Thermal ID**
Determines the size of the non-conductive void between the inner clad and outer plane.

**Thermal OD and Thermal OD-to-Hole Ratio**
**Thermal Outer Diameter** is the extent of the Thermal Pad Stack Layer and calculated as:
**Thermal ID Over Hole** + **Thermal OD Over ID** + (**Hole x Ratio**).

Example: Thermal OD = 0.40 + 0.30 + (0.70 x 1.1) = 1.47.

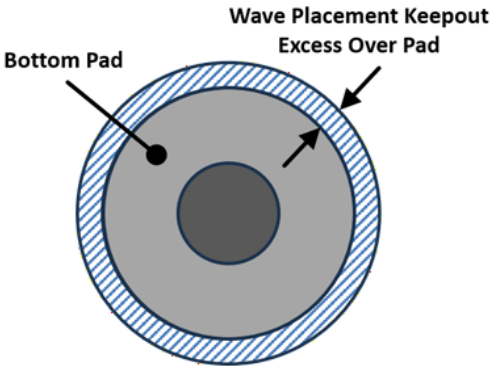
**Anti-pad**
An **Anti-pad** is a design feature that creates a plane clearance area around a plated or non-plated through-hole. The anti-pad void serves to avoid unintended connections between vias, traces and layers; improve solderability and reduce thermal stress during the assembly process. *In Footprint Expert, the Anti-pad is calculated to equal Thermal OD.*

**Thermal Spoke Width**

Width is calculated as:
**Spoke Width** = **Spoke Width %** x (**Thermal OD** / 4),
Example: Spoke Width = 0.75 x (1.47 / 4) = 0.28

**Wave Placement Keep-out Excess Over Pad**
A wave placement keep-out is a non-routable region on the bottom of a PC board that prevents solder from flowing into certain areas, such as component pads, mounting holes, fiducials or high-voltage zones during a wave soldering process.

The size of a Wave Placement Keep-out is completely up to the footprint designer based on a component's application. The size is simply defined as an excess to be added to the bottom pad.



# 10.0 – Courtyard Excess

In PCB design, courtyard excess refers to the specific clearance area between the combined physical boundary of a component (body and pads) and the outer boundary of its placement courtyard. This buffer zone ensures that components have sufficient space for manufacturing tolerances, mechanical assembly, and potential rework without interfering with neighboring parts.

Courtyards should not overlap in the part placement. Courtyards are used in a variety of ways in different CAD tools. The courtyard excess values are defined in the 3-Tier density levels for surface mount components.

- Least Density Level: 0.10 mm
- Nominal Density Level: 0.20 mm
- Most Density Level: 0.40 mm

The courtyard outline maps to the maximum package body dimensions and the pads.

For through-hole component footprints, the courtyard excess is set to a single value because through-hole technology only has a single density level. The typical through-hole courtyard excess is 0.25 mm.

**Requirements for Special Component Types**

While generic components follow standard density levels, certain parts require larger excess values due to their physical height or specialized assembly needs:

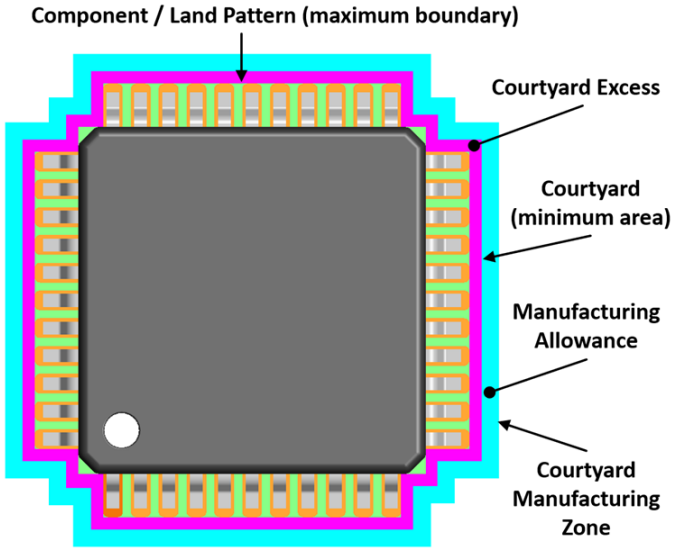
- **BGA/WLCSP Devices**: Typically require a **1.00 mm** clearance to allow for optical inspection of balls and specialized rework heat application.
- **Connectors**: Recommended excess is often **0.50 mm** to account for mating plug clearances and physical handling during insertion.
- **Tall Components**: Canned capacitors and crystals often utilize a **0.50 mm** excess to prevent tall bodies from shadowing or obstructing the placement of adjacent parts.
- **Large Non-Standard Packages**: For parts with any dimension over 10 mm, an excess of **0.50 mm** is often recommended to accommodate bulky rework equipment.

**Why Courtyard Excess is Critical**

- **Manufacturing Tolerances**: Accounts for registration errors during board fabrication and pick-and-place machine accuracy.
- **Rework Accessibility**: Provides enough room for tweezers, vacuum nozzles, or soldering iron tips to extract and replace a defective component without damaging neighbors.
- **Collision Prevention**: Ensures that the 3D bodies of components do not clash during automated assembly.
- **Solder Joint Inspection**: Allows sufficient visual or automated optical inspection (AOI) access to the solder fillets.

The courtyard excess for component body and footprint pads can be independently adjusted. The main reason for 2 different settings is because the physical package can move in any direction during reflow oven, but the pads never move. Typically, the courtyard to body and courtyard to pad are set to the same value for symmetry, but they can be adjusted to the individual user.

There is also a manufacturing allowance provided by the assembly shop as a courtyard-to-courtyard clearance rule. In the average case, courtyards can be bumped next to each other. But the assembly shop may provide a spacing rule between courtyards, and this is referred to as the manufacturing zone.




The original courtyard shape in IPC-SM-782 was rectangular. The contour courtyard was introduced in the IPC-7351 guideline. The Footprint Expert can automatically switch between either courtyard outline shape, and rebuild your entire library with whatever you choose.

# 11.0 – PCB Libraries Footprint Naming Convention – Surface Mount

Common package types and their respective naming conventions are listed below.

| | |
|---|---|
| Ball Grid Array's with Alphanumeric Rows | **BGA** + Pin Qty. + **C** or **N** + **P** Pitch _ Ball Columns **X** Ball Rows _ Body Length **X** Width **X** Height + **B** Ball Diameter |
| Ball Grid Array's with Alphanumeric Columns | **BGA** + Pin Qty. + **C** or **N** + **P** Pitch **+** A + Ball Columns **X** Ball Rows _ Body Length **X** Width **X** Height + **B** Ball Diameter |
| BGA w/Dual Pitch | **BGA** + Pin Qty. + **C** or **N** + **P** Col Pitch **X** Row Pitch _ Ball Columns **X** Ball Rows _ Body Length **X** Width **X** Height + **B** Ball Diameter |
| BGA w/Staggered Pins | **BGAS** + Pin Qty. + **C** or **N** + **P** Pitch _ Ball Columns **X** Ball Rows _ Body Length **X** Width **X** Height + **B** Ball Diameter |
| Capacitors, Aluminum Electrolytic | **CAPAE** + Base Body Size **X** Height + **L** Lead Length **X** Width |
| Capacitors, Chip, Array, Concave | **CAPCAV** + Pin Qty. + **P** Pitch _ + Body Length **X** Width **X** Height + **L** Lead Length **X** Width |
| Capacitors, Chip, Array, Flat | **CAPCAF** + Pin Qty. + **P** Pitch _ + Body Length **X** Width **X** Height + **L** Lead Length **X** Width |
| Capacitors, Chip | **CAPC** + Body Length **X** Width **X** Height + **L** Lead Length |
| Capacitors, Dual Flat No-lead | **CAPDFN** + Body Length **X** Width **X** Height + **L** Lead Length **X** Width |
| Capacitors, Molded | **CAPM** + Lead Span **X** Body Width **X** Height + **L** Lead Length **X** Width |
| Capacitors, Polarized, Chip | **CAPPC** + Body Length **X** Width **X** Height + **L** Lead Length |
| Capacitors, Polarized, Dual Flat No-lead | **CAPPDFN** + Body Length **X** Width **X** Height + **L** Lead Length **X** Width |
| Capacitors, Polarized, Molded | **CAPPM** + Lead Span **X** Body Width **X** Height + **L** Lead Length **X** Width |
| Capacitors, Side Concave, 2 Pin | **CAPSC** + Body Length **X** Width **X** Height + **L** Lead Length |
| Ceramic Flat Packages | **CFP** + Pin Qty. + **P** Pitch _ Body Length **X** Lead Span **X** Height + **L** Lead Length **X** Width |
| Column Grid Array, Circular Lead | **CGA** + Pin Qty. **P** Pitch _ Pin Columns **X** Pin Rows _ Body Length **X** Width **X** Height + **L** Diameter |
| Pillar Column Grid Array | **PCGA** + Pin Qty. **P** Pitch _ Pin Columns **X** Pin Rows _ Body Length **X** Width **X** Height + **L** Diameter |
| Crystals (2 leads) | **XTAL** + Body Length **X** Width **X** Height + **L** Lead Length **X** Width |
| Crystals, Dual Flat No-lead | **XTALDFN** + Body Length **X** Width **X** Height + **L** Lead Length **X** Width |
| Crystals, Side Concave | **XTALSC** + Body Length **X** Width **X** Height + **L** Lead Length |
| Diodes, Chip | **DIOC** + Body Length **X** Width **X** Height + **L** Lead Length |
| Diodes, Dual Flat No-lead | **DIODFN** + Pin Qty. _ Body Length **X** Width **X** Height + **L** Lead Length **X** Width |
| Diodes, Molded | **DIOM** + Lead Span **X** Body Width **X** Height + **L** Lead Length **X** Width |
| Diodes, Non-polarized, Chip | **DIONC** + Lead Span **X** Body Width **X** Height + **L** Lead Length |
| Diodes, Non-polarized, Dual Flat No-lead | **DIONDFN** + Pin Qty. _ Body Length **X** Width **X** Height + **L** Lead Length **X** Width |
| Diodes, Non-polarized, Molded | **DIONM** + Lead Span **X** Body Width **X** Height + **L** Lead Length **X** Width |
| Diodes, MELF | **DIOMELF** + Body Length + Diameter + **L** Lead Length |
| Diodes, Side Concave | **DIOSC +** Body Length **X** Width **X** Height + **L** Lead Length |
| Diodes, Side Concave, 4 Pin | **DIOSC4** + **P** Pitch _ Body Length **X** Width **X** Height + **L** Lead Length |
| Diodes, Small Outline Flat Lead, 2 Pin | **SODFL** + Lead Span **X** Body Width **X** Height + **L** Lead Length **X** Width |
| Diodes, Small Outline Flat Lead, 3 - 6 Pin | **DIOSOFL** + Pin Qty. + **P** Pitch _ + Lead Span **X** Body Height + **L** Lead Length **X** Width |
| DPAK | **DPAK** + Pin Qty. + **P** Pitch _ Lead Span **X** Height + **L** Lead Length **X** Width + **T** Thermal Tab Pad Length **X** Width |
| Ferrite Bead, Chip | **BEADC** + Body Length **X** Width **X** Height + **L** Lead Length |

| | |
|---|---|
| Fuses, Chip | **FUSC** + Body Length **X** Width **X** Height + **L** Lead Length |
| Fuses, Dual Flat No-Lead | **FUSDFN** + Body Length **X** Width **X** Height + **L** Lead Length **X** Lead Width |
| Fuses, Molded | **FUSM** + Lead Span **X** Body Width **X** Height + **L** Lead Length **X** Lead Width |
| Fuses, Side Concave | **FUSSC** + Body Length **X** Width **X** Height + **L** Lead Length |
| IC, Small Outline Package, Flat Lead | **SOPFL** + Pin Qty. + **P** Pitch _ + Lead Span **X** Body Height + **L** Lead Length **X** Width |
| Inductors, Chip | **INDC** + Body Length **X** Width **X** Height + **L** Lead Length |
| Inductors, Chip, Array, Concave | **INDCAV** + Pin Qty. + **P** Pitch _ Body Length **X** Width **X** Height + **L** Lead Length **X** Width |
| Inductors, Chip, Array, Flat | **INDCAF** + Pin Qty. + **P** Pitch _ Body Length **X** Width **X** Height + **L** Lead Length **X** Width |
| Inductors, Dual Flat No-lead | **INDDFN** + Body Length **X** Width **X** Height + **L** Lead Length **X** Width |
| Inductors, Molded | **INDM** + Lead Span **X** Body Width **X** Height + **L** Lead Length **X** Width |
| Inductors, Precision, Molded | **INDPM** + Lead Span **X** Body Width **X** Height + **L** Lead Length **X** Width |
| Inductors, Side Concave | **INDSC** + Body Length **X** Width **X** Height + **L** Lead Length |
| Integrated Circuit, Small Outline, Flat Lead, 3 - 6 pin | **ICSOFL** + Pin Qty. + **P** Pitch _ + Lead Span **X** Body Height + **L** Lead Length **X** Width |
| Land Grid Array, Circular Lead | **LGA** + Pin Qty. + **C** + **P** Pitch _ Pin Columns **X** Pin Rows _ Body Length **X** Width **X** Height + **L** Lead Diameter |
| Land Grid Array, Square Lead | **LGA** + Pin Qty. + **S** + **P** Pitch _ Pin Columns **X** Pin Rows _ Body Length **X** Width **X** Height + **L** Lead Size |
| LED's, Chip | **LEDC** + Body Length + Width **X** Height + **L** Lead Length |
| LED's, Dual Flat No-lead | **LEDDFN** + Body Length **X** Width **X** Height + **L** Lead Length **X** Width |
| LED's, Molded | **LEDM** + Lead Span **X** Body Width **X** Height + **L** Lead Length **X** Width |
| LED's, Side Concave | **LEDSC** + Body Length **X** Width **X** Height + **L** Lead Length |
| LED's, Side Concave, 4 Pin | **LEDSC4** + **P** Pitch _ Body Length **X** Width **X** Height + **L** Lead Length |
| Oscillators, Dual Flat No-Lead (4-pin) | **OSCDFN4** _ Body Length **X** Width **X** Height + **L** Lead Length **X** Width |
| Oscillators, Side Concave | **OSCSC** + Pin Qty. + **P** Pitch _ Body Length **X** Width **X** Height + **L** Lead Length **X** Width |
| Oscillators, Side Flat | **OSCSF** + Pin Qty. + **P** Pitch _ Body Length **X** Width **X** Height + **L** Lead Length **X** Width |
| Oscillators, J-Lead | **OSCJ** + Pin Qty. + **P** Pitch _ Body Length **X** Lead Span **X** Height + **L** Lead Width |
| Oscillators, L-Bend Lead | **OSCL** + Pin Qty. + **P** Pitch _ Body Length **X** Lead Span **X** Height + **L** Lead Length **X** Width |
| Oscillators, Corner Concave | **OSCCC** + Body Length **X** Width **X** Height + **L** Lead Length **X** Width |
| Plastic Leaded Chip Carriers | **PLCC** + Pin Qty. + **P** Pitch _ Lead Span L1 **X** Lead Span L2 Nominal **X** Height + **L** Lead Width |
| Plastic Leaded Chip Carrier Sockets Square | **PLCCS** + Pin Qty. + **P** Pitch _ Lead Span L1 **X** Lead Span L2 Nominal **X** Height + **L** Lead Width |
| Pull-back Small Outline No-lead | **PSON** + Pin Qty. + **P** Pitch _ Body Length **X** Width **X** Height + **L** Lead Length **X** Width + **T** Thermal Pad Length **X** Width |
| Pull-back Quad Flat No-lead | **PQFN** + Pin Qty. + **P** Pitch _ Body Length **X** Width **X** Height + **L** Lead Length **X** Width + **T** Thermal Pad Length X Width |
| Quad Flat Packages | **QFP** + Pin Qty. + **P** Pitch _ Lead Span L1 **X** Lead Span L2 Nominal **X** Height + **L** Lead Length **X** Width + **T** Thermal Pad Length X Width |
| Ceramic Quad Flat Packages | **CQFP** + Pin Qty. + **P** Pitch _ Lead Span L1 **X** Lead Span L2 Nominal **X** Height + **L** Lead Length X Width |
| Quad Flat No-lead | **QFN** + Pin Qty. + **P** Pitch _ Body Length **X** Width **X** Height + **L** Lead Length **X** Width + **T** Thermal Pad Length X Width |

| | |
|---|---|
| Quad Leadless Ceramic Chip Carriers | **LCC** + Pin Qty. + **P** Pitch _ Body Length **X** Width **X** Height + **L** Lead Length **X** Width |
| Quad Leadless Ceramic Chip Carriers (Pin 1 on Side) | **LCCS** + Pin Qty. + **P** Pitch _ Body Length **X** Width **X** Height + **L** Lead Length **X** Width |
| Resistors, Chip | **RESC** + Body Length **X** Width **X** Height + **L** Lead Width |
| Resistors, Chip, Array, Concave | **RESCAV** + Pin Qty. + **P** Pitch _ Body Length **X** Width **X** Height + **L** Lead Length **X** Width |
| Resistors, Chip, Array, Convex, E-Version (Even Pin Size) | **RESCAXE** + Pin Qty. + **P** Pitch _ Body Length **X** Width **X** Height + **L** Lead Length **X** Width |
| Resistors, Chip, Array, Convex, S-Version (Side Pins Diff) | **RESCAXS** + Pin Qty. + **P** Pitch _ Body Length **X** Width **X** Height + **L** Lead Length **X** Width |
| Resistors, Chip, Array, Flat | **RESCAF** + Pin Qty. + **P** Pitch _ Body Length **X** Width **X** Height + **L** Lead Length **X** Width |
| Resistors, Dual Flat No-lead | **RESDFN** + Pin Qty. _ Body Length **X** Width **X** Height + **L** Lead Length **X** Width |
| Resistors, MELF | **RESMELF** + Body Length + Diameter + **L** Lead Width |
| Resistors, Molded | **RESM** + Lead Span **X** Body Width **X** Height + **L** Lead Length **X** Width |
| Resistors, Side Concave | **RESSC** + Body Length **X** Width **X** Height + **L** Lead Length **X** Width |
| Small Outline IC, J-Leaded | **SOJ** + Pin Qty. + **P** Pitch _ Body Length **X** Lead Span **X** Height + **L** Lead Width |
| Small Outline IC, L-Leaded | **SOL** + Pin Qty. + **P** Pitch _ Body Length **X** Lead Span **X** Height + **L** Lead Width |
| Small Outline Integrated Circuit, (50 mil Pitch SOIC) | **SOIC** + Pin Qty. + **P** Pitch _ Body Length **X** Lead Span **X** Height + **L** Lead Length **X** Width |
| Small Outline Packages | **SOP** + Pin Qty. + **P** Pitch _ Body Length **X** Lead Span **X** Body Height + **L** Lead Length **X** Width + **T** Thermal Pad Length **X** Width |
| Small Outline No-lead | **SON** + Pin Qty. + **P** Pitch _ Body Length **X** Width **X** Height + **L** Lead Length **X** Width + **T** Thermal Pad Length **X** Width |
| Small Outline Diode | **SOD** + Lead Span **X** Body Width **X** Height + **L** Lead Length **X** Width |
| SOT143 | **SOT143** + **P** Pitch _ Body Length **X** Lead Span **X** Body Height + **L** Lead Length |
| SOT223 | **SOT223** + Pin Qty. + **P** Pitch _ Body Length **X** Lead Span **X** Body Height + **L** Lead Length |
| Thermistors, Chip | **THRMC** + Body Length + Width **X** Height + **L** Lead Width |
| Transistors, Small Outline, Flat Lead, 3 - 6 pin | **TRXSOFL** + Pin Qty. + **P** Pitch _ + Lead Span **X** Body Length **X** Body Height + **L** Lead Length **X** Width |
| Transistors, Dual Flat No-lead | **TRXDFN** + Pin Qty. _ Body Length **X** Body Width **X** Height + **L** Lead Length **X** Width |
| Varistors, Chip | **VARC** + Body Length **X** Width **X** Height + **L** Lead Width |

**SOT23 Form Factor Packages (EIA SOT & JEITA SC)**

| | |
|---|---|
| SOT23-3 | **SOT23-3P95** _ Body Length **X** Lead Span **X** Body Height + **L** Lead Length |
| SC59-3 | **SC59-3P95** _ Body Length **X** Lead Span **X** Body Height + **L** Lead Length |
| SOT23-5 | **SOT23-5P95** _ Body Length **X** Lead Span **X** Body Height + **L** Lead Length |
| SC59-5 | **SC59-5P95** _ Body Length **X** Lead Span **X** Body Height + **L** Lead Length |
| SOT23-6 | **SOT23-6P95** _ Body Length **X** Lead Span **X** Body Height + **L** Lead Length |
| SC74 | **SC74-6P95** _ Body Length **X** Lead Span **X** Body Height + **L** Lead Length |
| SOT28 | **SOT28-8P65** _ Body Length **X** Lead Span **X** Body Height + **L** Lead Length |
| SC70-8 | **SC70-8P65** _ Body Length **X** Lead Span **X** Body Height + **L** Lead Length |
| SOT323 | **SOT323-3P65** _ Body Length **X** Lead Span **X** Body Height + **L** Lead Length |
| SC70 | **SC70-3P65** _ Body Length **X** Lead Span **X** Body Height + **L** Lead Length |
| SOT346 | **SOT346-3P95** _ Body Length **X** Lead Span **X** Body Height + **L** Lead Length |
| SC59A | **SC59-3P95** _ Body Length **X** Lead Span **X** Body Height + **L** Lead Length |
| SOT346T | **SOT346T-3P95** _ Body Length **X** Lead Span **X** Body Height + **L** Lead Length |
| SC96 | **SC96-3P95** _ Body Length **X** Lead Span **X** Body Height + **L** Lead Length |
| SOT353 | **SOT353 -5P65** _ Body Length **X** Lead Span **X** Body Height + **L** Lead Length |
| SC88A | **SC88A-5P65** _ Body Length **X** Lead Span **X** Body Height + **L** Lead Length |
| SOT363 | **SOT363-6P65** _ Body Length **X** Lead Span **X** Body Height + **L** Lead Length |
| SC88 | **SC88-6P65** _ Body Length **X** Lead Span **X** Body Height + **L** Lead Length |
| SOT416 | **SOT416-3P50** _ Body Length **X** Lead Span **X** Body Height + **L** Lead Length |
| SC75 | **SC75-3P50** _ Body Length **X** Lead Span **X** Body Height + **L** Lead Length |
| SOT753 | **SOT753 -5P95** _ Body Length **X** Lead Span **X** Body Height + **L** Lead Length |
| SC74A | **SC74A-5P95** _ Body Length **X** Lead Span **X** Body Height + **L** Lead Length |

**Note: All footprint dimensional values are Nominal except Height is Maximum**

All dimensions are in Metric Units
All Lead Span and Height numbers go two places past the decimal point and “include” trailing Zeros
All Lead Span and Body Sizes go two place before the decimal point and “remove” leading Zeros
All Chip Component Body Sizes are one place to each side of the decimal point
Pitch Values are two places to the right & left of decimal point with no leading Zeros but include trailing zeros

**Land Pattern Naming Convention:** Each land pattern in IPC-7351 is specified by a unique name that must convey the package family type, pin quantity, pin pitch, body length and width dimensions, terminal lead span, terminal lead length and width and thermal pad dimensions whenever applicable. Other fields in a land pattern name are optional and are discussed below.

The following notes provide guidance on using the tables above. Specific characters are reserved for use in the naming convention to denote or separate certain fields:

- **P** : Prefixes pin pitch. For example, P80 specifies a 0.80 mm pitch between terminations.
- **L** : Prefixes nominal lead dimensions
- **T** : Prefixes thermal tab dimensions
- **X** : Dimension separator. For example, 0.80 mm by 1.50 mm is denoted 80X150
- **C, N** : Denote Collapsing and Non-collapsing balls respectively when specifying a BGA land pattern
- _: Underscore is a field separator between pin quantity and/or pin pitch and the package body dimensions
- **-**: Dash is a field separator between pin quantity in hidden and deleted pin components
- **+** : Plus denotes "in addition to". The plus "+" symbol does not actually appear in the land pattern name, it is only used to assist in reading the information.

**Additional notes**:

- All dimensions are metric units
- All dimensions are nominal except height is maximum
- All numeric values are two places before and after the decimal point and “remove” leading Zeros
- If there is no pin quantity in the Land Pattern Name it is assumed that the pin quantity is 2
- Thermal Tabs are included in the Pin Quantity

**Additional and Optional Fields**:
The suffix letters “L”, “M”, and “N” are used to signify when the land protrusion is at their minimum (least), maximum (most), or median (nominal) protrusion and appear as the last character. The 3 Density Levels are defined as follows:

- M = Maximum (Most) Material Condition (Density Level A)
- N = Median (Nominal) Material Condition (Density Level B)
- L = Minimum (Least) Material Condition (Density Level C)

If no Density Level suffix is provided, then the land pattern either follows the component manufacturer's recommended pattern or a custom land pattern for use with multiple component manufacturer’s packages in the same component family.

Additional suffices for JEDEC Standard parts that have several alternate packages are as follows:
AA, AB, AC JEDEC Component Identifier (used primarily on Semiconductor packages).

Additional suffixes for alternate components that do not follow the JEDEC standard are as follows (these are located before the Density Level suffix):

“A” – Alternate Component letter is used when component package nominal dimensions are the same for two packages but the package tolerances are different enough to create a unique land pattern to avoid land pattern name duplication.

Ball Grid Array (BGA) packages may require land pattern names that indicate a difference in pitch between balls in the rows vs. balls in the columns. These are often referred to as a “dual pitch BGA”. For example, the BGA land pattern name of BGA48C**80X100**P6X8_900X1200X120 conveys that the pitch 0.80 mm between columns and 0.10 mm between rows.
Note: In this example, Pin A1 is assumed to be located in the Lower left when viewing the package from the top view. A 90 rotation of the BGA swaps the definition of Rows and Columns.

A pin order or pin quantity modifier shall be added to the component package type specification to convey reverse pin ordering, hidden pins, or deleted pins.

- **SOP20R:** 20 pin part, Reverse Pin Order
- **SOT143R**: Reverse Pin Order
- **SOP20-24**: 20 pin part in a 24 pin package. The pins are numbered 1 – 24 the hidden pins are skipped over. The schematic symbol displays up to 24 pins.
- **SOP24-20**: 20 pin part in a 24 pin package. The pins are numbered 1 – 20 the deleted pins are removed. The schematic symbol displays 20 pins.

**Land Pattern Naming for Non-conforming Packages:** A large number of component packages are unique, non-standard packages or unique connectors. These component packages do not fit into a standard land pattern name due to their unique features. Therefore, in order to have a single land pat tern naming convention that covers every component package in the electronics industry, the land pattern name must be associated with the component manufacturer and their part number or case code as shown below:

ManufacturerNameAbbreviation_ManufacturerPartNumber or
ManufacturerNameAbbreviation_ManufacturerCaseCode

All special characters used in the part number will be replaced with a hyphen "-" except periods "." will be replaced with an underscore "_".

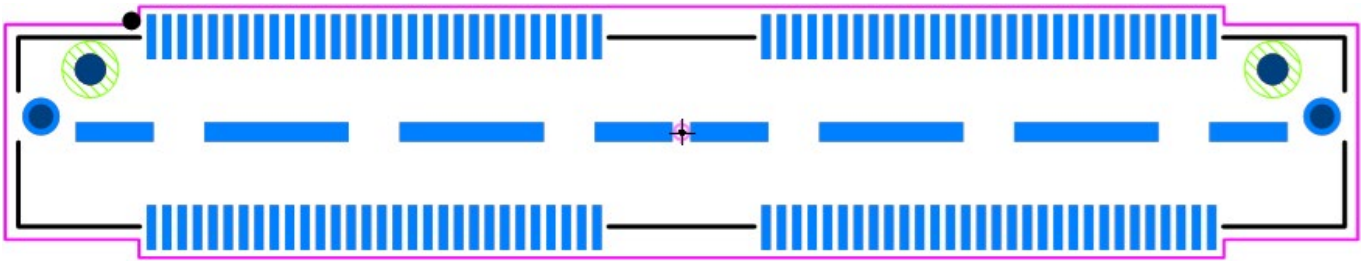
If the component package or connector is unique and has a single manufacturer part number, then **Part Number** would be used to generate the Land Pattern Name
The component is a standard package and is associated with multiple manufacturer part numbers then manufacturer **Case Code** would be used to generate the Land Pattern Name

**Examples:**

| | | |
|---|---|---|
| FOXCONN_JFM38U1A-2PVT-4F | TI_RKG41 | CK_CRD16CM0SB |
| MOLEX_67503-1020 | MAXIM_L1053-H2 | ABRACON_ABM11 |
| SAMTEC_QTH-060-01-L-D-A | CUI_SJ-3566AN | AMPHENOL_101-00565-64 |

For reference, various unique footprints are shown below that are non-conforming with Tables above.

This is the footprint of SAMTEC_QTH-060-01-L-D-A, an connector with plated mounting and non-plated alignment holes.



# 12.0 – IPC-7352 Footprint Naming Convention – Through-hole

The land pattern naming convention uses component dimensions to derive the land pattern name.
The first 3 - 6 characters in the land pattern name describe the component family.
The first number in the land pattern name refers to the Lead Spacing or hole to hole location to insert the component lead.
All numbers that follow the Lead Spacing are component dimensions.

These characters are used as component body identifiers that precede the value and this is the priority order of the component body identifiers –

- **P** = Pitch for components with more than two leads
- **W** = Maximum Lead Width (or Component Lead Diameter)
- **L** = Body Length for horizontal mounting
- **D** = Body Diameter for round component body
- **T** = Body Thickness for rectangular component body
- **H** = Height for vertically mounted components
- **Q** = Pin Quantity for components with more than two leads
- **R** = Number of Rows for connectors

Notes:
All component body values are in millimeters and go two places to the right of the decimal point and no leading zeros.
All Complexity Levels used in the examples are "**B**".

| Component, Category | Land Pattern Name |
|---|---|
| Capacitors, Non-Polarized Axial Diameter Horizontal Mounting | **CAPAD** + Lead Spacing + **W** Lead Width + **L** Body Length + **D** Body Diameter |
| Capacitors, Non-Polarized Axial Rectangular | **CAPAR** + Lead Spacing + **W** Lead Width + **L** Body Length + **T** Body thickness + **H** Body Height |
| Capacitors, Non-Polarized Axial Diameter Vertical Mounting | **CAPADV** + Lead Spacing + **W** Lead Width + **L** Body Length + **D** Body Diameter |
| Capacitors, Non-Polarized Axial Rect. Vert. Mtg. | **CAPARV** + Lead Spacing + **W** Lead Width + **L** Body Length + **T** Body Thickness + **H** Body Height |
| Capacitors, Non-Polarized Radial Diameter | **CAPRD** + Lead Spacing + **W** Lead Width + **D** Body Diameter + **H** Body Height |
| Capacitors, Non-Polarized Radial Rectangular | **CAPRR** + Lead Spacing + **W** Lead Width + **L** Body Length + **T** Body thickness + **H** Body Height |
| Capacitors, Non-Polarized Radial Disk Button | **CAPRB** + Lead Spacing + **W** Lead Width + **L** Body Length + **T** Body thickness + **H** Body Height |
| Capacitors, Polarized Axial Diameter Horizontal Mounting | **CAPPAD** + Lead Spacing + **W** Lead Width + **L** Body Length + **D** Body Diameter |
| Capacitor, Polarized Radial Diameter | **CAPPRD** + Lead Spacing + **W** Lead Width + **D** Body Diameter + **H** Body Height |
| Diodes, Axial Diameter Horizontal Mounting | **DIOAD** + Lead Spacing + **W** Lead Width + **L** Body Length + **D** Body Diameter |
| Diodes, Axial Diameter Vertical Mounting | **DIOADV** + Lead Spacing + **W** Lead Width + **L** Body Length + **D** Body Diameter |
| Dual-In-Line Packages | **DIP** + Lead Span + **W** Lead Width + **P** Pin Pitch + **L** Body Length + **H** Component Height + **Q** Pin Qty |
| Dual-In-Line Sockets | **DIPS** + Lead Span + **W** Lead Width + **P** Pin Pitch + **L** Body Length + **H** Component Height + **Q** Pin Qty |
| Headers, Vertical | **HDRV** + Lead Span + **W** Lead Width + **P** Pin Pitch + **R** Pins per Row + **L** Body Length + **T** Body Thickness + **H** Height |
| Headers, Right Angle | **HDRRA** + Lead Span + **W** Lead Width + **P** Pin Pitch + **R** Pins per Row + **L** Body Length + **T** Body Thickness + **H** Height |
| Inductors, Axial Diameter Horizontal Mounting | **INDAD** + Lead Spacing + **W** Lead Width + **L** Body Length + **D** Body Diameter |
| Inductors, Axial Diameter Vertical Mounting | **INDADV** + Lead Spacing + **W** Lead Width + **L** Body Length + **D** Body Diameter |
| Inductors, Non-Polarized, Radial Diameter | **INDRD** + Lead Spacing + **W** Lead Width + **D** Body Diameter + **H** Body Height |
| Inductors, Polarized, Radial Diameter | **INDPRD** + Lead Spacing + **W** Lead Width + **D** Body Diameter + **H** Body Height |

| | |
|---|---|
| Jumpers, Wire | **JUMP** + Lead Spacing + **W** Lead Width |
| Mounting Holes Plated with Support Pad | **MTGP** + Pad Size + **H** Hole Size + **Z** Inner Layer Pad Size |
| Mounting Holes Non-Plated With Support Pad | **MTGNP** + Pad Size + **H** Hole Size + **Z** Inner Layer Pad Size |
| Mounting Holes Non-Plated Without Support Pad | **MTGNP** + Pad Size + **H** Hole Size + **Z** Inner Layer Pad Size + **K** Keep-out Diameter |
| Mounting Holes Plated with 8 Vias | **MTGP** + Pad Size + **H** Hole Size + **Z** Inner Layer Pad Size + 8 Vias |
| Pin Grid Array's | **PGA** + Pin Qty + **P** Pitch + **C** Pin Columns + **R** Pin Rows + **L** Body Length **X** Body Width + **H** Component Height |
| Resistors, Axial Diameter Horizontal Mounting | **RESAD** + Lead Spacing + **W** Lead Width + **L** Body Length + **D** Body Diameter |
| Resistors, Axial Diameter Vertical Mounting | **RESADV** + Lead Spacing + **W** Lead Width + **L** Body Length + **D** Body Diameter |
| Resistors, Axial Rectangular Horizontal Mounting | **RESAR** + Lead Spacing + **W** Lead Width + **L** Body Length + **T** Body thickness + **H** Body Height |
| Single-In-Line Packages | **SIP** + Body Width + **W** Lead Width + **P** Pin Pitch + **L** Body Length + **H** Component Height + **Q** Pin Qty |
| Test Points, Round Land | **TP** + Lead Width |
| Test Points, Square Land | **TPS** + Lead Width |
| Test Points, Top Land Round & Bottom Land Square | **TPRS** + Lead Width |
| Wire | **PAD** + Wire Width |

# 13.0 – IPC-7352 Pad Stack Naming Convention

The pad stack consists of combinations of letters and numbers that represent shape, or dimensions of lands on different layers of printed boards or documentation. The name of the pad stack needs to represent all the various combinations. These are used in combination with the land pattern conventions defined herein according to the rules established in the IPC-2220 Design standards.

All dimensions in this Naming Convention section are in “mm”, unless otherwise noted.

The first part of the pad stack convention consists of a land shape. There are ten basic land shape identifiers. Note: All alphabetical characters are “lower case”. This helps discriminate numeric values.

**Basic Land Shape Letters**

1. **r** = Rectangle
2. **rr** = Rounded Rectangle
3. **cr** = Chamfered Rectangle
4. **b** = Oblong
5. **d** = D Shape (Square on one end and Circular on the other end)
6. **c** = Circular
7. **s** = Square
8. **rs** = Rounded Square
9. **cs** = Chamfered Square
10. **u** = User Defined Contour (Irregular Shape)

**Pad Stack Defaults**

- Solder Mask is 1:1 scale of the land size
- Paste Mask is 1:1 scale of the land size
- The Assembly Layer land is 1:1 scale of the land size
- Inner Layer Land is the same shape as the outer layer land
- The Primary and Secondary lands are the same size
- The inner layer land shapes are Circular
- Vias are Circular
- Thermal ID, OD and Spoke Width sizes follow the IPC Level A, B or C
- Plane Clearance Anti-pad size follows the IPC Level A, B or C
- Thermals have 4 spokes
- Mounting Holes are Circular

Note: Every board fabricator’s ability to register solder mask is different. The 1:1 scale solder mask covers the variation, and so long as manufacturers are building to specs such as IPC-6012 that say you can’t have mis-registration of the solder mask.

Illegal characters that cannot be used (Microsoft requirement) include “ ” , ; : / \ [ ] ( ) . { } * & % # $ ! @ ^ =

Examples utilizing the pad stack naming convention (all values are in metric units)
Note: Every number goes two places to the right and as many as needed to the left of the decimal

Examples: 1150 = 11.50 or 11500 µm, 150 = 1.50 or 1500 µm, 15 = 0.15 or 150 µm

- **c150h90** where "**c**" denotes a Circular land with a 1.50 diameter and H denotes a hole size of 0.90
- **c130_95** Donut pad where "**c**" denotes a Circular land with a 1.30 OD diameter and 95 denotes the ID diameter
- **c130_95hn70k147** Donut pad - "**c**" denotes a Circular land with a 1.30 OD diameter and 95 denotes the ID diameter and hn70 denotes hole, non-plated 0.70 diameter and k147 denotes a keep-out 1.47 diameter
- **v50h25** where a "**v**" denotes a via with a 0.50 land (default Circular land) and h denotes a 0.25 hole
- **s150h90** where "**s**" denotes a 1.50 Square land and h denotes a hole size of 0.90
- **s350** where "**s**" denotes a square SMT land size of 3.50
- **r200_100** where "**r**" denotes a Rectangular SMT land 2.00 land length X 1.00 land width
- **b300_150** where "**b**" denotes a SMT Oblong land size of 3.00 X 1.50
- **b400_200h100** where "**b**" denotes an Oblong land size of 4.00 length X 2.00 width and 1.00 hole
- **d300_150** where "**d**" denotes land with one circular end and one square end (looks like a D) 3.00 X 1.50
- **v30h15l1-3** where "**v**" denotes a 0.30 blind via with 0.15 Hole; 1 is the starting layer, 3 is the end layer
- **r200_100r5** = Rounded Rectangular 2.00 X 1.00 X 0.05 radius corners
- **r200_100c10** = Chamfered Rectangular 2.00 X 1.00 X 0.10 chamfered corners
- **v30h15l3-6** where "**v**" denotes a 0.30 buried via with 0.15 Hole; 3 is the starting layer, 6 is the end layer

Note: It is assumed that the through-hole pad stack has the same value as the mounted layer size and shape for –

- Inner Layer
- Opposite Side
- Solder Mask
- Solder Paste
- Assembly Layers

It is also assumed that the "Plane Clearance" and "Thermal Relief" data follows the through-hole convention guidelines defined in the IPC-2221 and IPC-2222 standards.

Modifiers that are used when pad stack features are different than the defaults

These are the "Variants" or "Modifiers" that go after the basic pad stack naming convention.
These are used when the User needs to change the pad stack default values either by a different dimension or a different shape. In instances where shapes are different this becomes a two letter code with the modifier first followed by the land shape letter.

- **n** = Non-plated Hole
- **z** = Inner Layer land dimension if different than the land on primary layer
- **x** = Special modifier used alone or following other modifiers for lands on opposite side to primary layer land dimension
- **t** = Thermal Relief; if different than IPC standard pad stack – tid_od_sw for 4 spoke default
- **m** = Solder Mask if different than default 1:1 scale of land
- **p** = Solder Paste if different than default 1:1 scale of land
- **a** = Assembly surface land if different than default 1:1 scale of land
- **y** = Plane Clearance (Anti-pad) if the value is different than the Thermal OD
- **o** = Offset Pad & Solder Mask with the same + / - value
- **om** = Offset Solder Mask Only + / - value
- **op** = Offset Paste Mask only + / - value
- **k** = Keep-out
- **r** = Radius for Rounded Rectangular Land Shape
- **c** = Chamfer for Chamfered Rectangular Land Shape

Shape change is the last letter in the string prior to the dimension.

**Other usage of the pad stack naming convention**

**USE of letter v:** Vias can be named using the pad stack naming convention. Because most vias use lands that are circular in shape, the letter "**v**" will be used in place of the letter "**c**" in the pad stack naming convention. If this is not true the modifiers can be added after the letter "**v**" to signify shape or dimensional changes to this default.

**USE of letter w:** In addition to Vias the pad stack naming convention can also be used for defining mounting holes. The letter "**w**" shall be used to define the mounting hole characteristics and any associated lands used for the surface lands (either plated or un-plated)

**Examples of double character modifiers:**

- **ts** = Thermal Square; if different than the top side land shape and dimensions
- **sw** = Thermal spoke width
- **zs** = Inner Layer Land Shape is Square (Note: The default is circular)
- **m0** = No Solder Mask
- **mxc** = Solder Mask Opposite Side Circular
- **mx0** = Solder Mask Opposite Side No Solder Mask
- **p0** = No Paste Mask
- **xc** = Opposite Side Circular
- **vs** = Via with Square land
- **hn** = Non-plated Hole

**Modifier Example for Through-hole:**

- **s150h90zs150** = where "s" is Square 1.50 land with 0.90 Hole with 1.50 inner (Z) Layer Square land
- **c150h90zc150** = where "c" is Circular 1.50 land with 0.90 Hole with 1.50 inner (Z) Layer Circular land

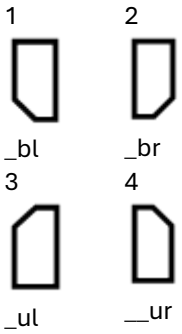
**Modifier Examples for Vias:**

- **vs50h25** where "vs" denotes a 0.50 Square Via with a 0.25 Hole
- **v50h25xs70** where "v" is 0.50 Circular Via with 0.25 Hole and 0.70 Square land on opposite side

Chamfered & Rounded corner modifiers are used to indicate which corner(s) are modified.
Order of precedence has been given to the first 4 modifiers.

**Modifiers:**

- **bl** – bottom left
- **br** – bottom right
- **ul** – upper left
- **ur** – upper right
- **ulr** – upper left & right
- **blr** – bottom left & right
- **ubl** – upper and bottom left
- **ubr** – upper and bottom right




**Rounded and Chamfered lands in "one corner" Modifier Examples:**

- **r100_200rbl50** = rectangular land 1.00 x 2.00 with 0.50 radius for rounded corner in bottom left corner
- **r100_200rbr50** = rectangular land 1.00 x 2.00 with 0.50 radius for rounded corner in bottom right corner
- **r100_200rul50** = rectangular land 1.00 x 2.00 with 0.50 radius for rounded corner in upper left corner
- **r100_200rur50** = rectangular land 1.00 x 2.00 with 0.50 radius for rounded corner in upper right corner
- **r100_200cbl50** = rectangular land 1.00 x 2.00 with 0.50 chamfer for chamfer corner in bottom left corner
- **r100_200cbr50** = rectangular land 1.00 x 2.00 with 0.50 chamfer for chamfer corner in bottom right corne
- **r100_200cul50** = rectangular land 1.00 x 2.00 with 0.50 chamfer for chamfer corner in upper left corner
- **r100_200cur50** = rectangular land 1.00 x 2.00 with 0.50 chamfer for chamfer corner in upper right corner

**Examples of a square land with 3 rounded and 1 chamfered corner (for Thermal Pad)**

- **s300p190r25cul50** = square 3.00 land, square paste 1.90, corner radius 0.25, upper-left chamfer 0.50
- **s300p190r25cbl50** = square 3.00 land, square paste 1.90, corner radius 0.25, bottom-left chamfer 0.50

Chamfered and Rounded Rectangular with all four corners chamfered does not need a corner modifier.
Modifier Examples with Rounded Rectangle Land Shape:

- **r200_100r50** = rectangular land 2.00 x 1.00 with 0.50 radius for rounded corners in all 4 corners
- **r200_100c50** = rectangular land 2.00 x 1.00 with 0.50 chamfer for chamfered corners in all 4 corners

**Examples of a pad stack with Circular land with hole using various modifiers**

- **c150h90** = Default pad stack with a 1.50 circular land with a 0.90 hole (no modifiers used)
- **c150hn90** = Default pad stack with a 1.50 circular land with a 0.90 non-plated hole (no modifiers used)
- **c150h90z140** = Inner layer land is smaller than external lands 1.40 or 0.10 smaller
- **c150h90z140x170** = Opposite side land is larger than top side land 1.70 or 0.20 larger
- **c150h90z140x170m165mx185** = Solder mask opening for top and bottom lands 0.15 larger for each
- **c150h90z140x170m165mX185a200** = Assembly drawing land in 0.50 larger than 1.50 primary land
- **c150h90z140x170m165mx185a200y300** = Plane clearance anti-pad diameter is 3.00
- **c150h90z140x170m165mx85** = Solder mask encroachment on opposite land by 0.65 smaller
- **c150h90m165** = adding a solder mask opening of 1.65 diameter or 0.15 larger than land
- **c150h90t150_180_40** = Thermal ID 1.50, OD 1.80, Spoke Width 0.40, Anti-pad 1.80
- **c150h90t150_180_40y200** = Anti-pad 2.00 (because the size is different than the Thermal OD)
- **c150h90t150_180_80_2** = Spoke Width 0.80 with 2 Spokes
- **c150h90m165t150_180_40** = Solder Mask 1.65

**Examples of a pad stack with Oblong land with Slotted Hole**

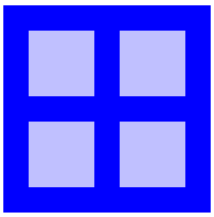
- **Sample – b** = Oblong Land Shape then "**X**" dimension (length) then Underscore _ "**Y**" dimension (width)
- **b400_200h300_100** = Oblong land 4 length X 2 width with slotted hole size 3 X 1
- **b400_200hn300_100** = Oblong land 4 X 2 with non-plated slotted hole size 3 X 1

**Examples of a SMT pad stack land using various modifiers**

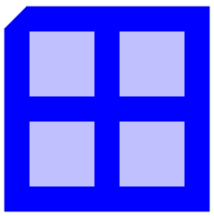
- **b300_150** = Default pad stack with a 3.00 length and 1.50 width land (no modifiers used)
- **b300_150m330_180** = Solder Mask is 0.30 larger than the land on all sides
- **b300_150m330_180p240_140** = Solder Paste is smaller by 0.10 width and 0.60 length
- **b300_150b-50** = Oblong Land 3.00 X 1.50 w/Offset Origin negative 0.50
- **r400_200pb430_230** = Rectangle SMT land 4.00 X 2.00 with an Oblong Paste Mask size of 4.30 X 2.30

## Example of Thermal Pads for QFN, SON, QFP and SOP

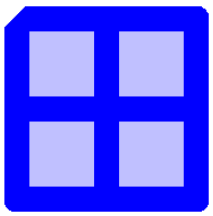
### Square Configurations



**s480p4s152** = 4.80 Square Land with 4 Paste Mask Squares 1.52 each



**s480p4s152cul50** = 4.80 Square Land with 4 Paste Mask Squares 1.52 each with 0.50 Chamfer in Upper Left corner



**s480p4s152cul50r25** = 4.80 Square Land with 4 Paste Mask Squares 1.52 each with 0.50 Chamfer in Upper Left corner with 0.25 corner Radius

## Example of a Mounting Hole

- **w700h400z520m720** = This is a Plated Through Mounting hole for a #6-32 screw using a 4.00 diameter hole and having a circular 7.00 land on the primary and secondary side of the board, with a solder mask clearance that is 0.20 larger than the 7.20 land. The internal lands are smaller that the external and are also circular 5.20 in diameter.
- **w700hn400z520m720** = Non-plated version

## Example of a Local Fiducial for Fine Pitch SMT Components

- **c100m200k200** = Circular Land 1.00 with Solder Mask 2.00 with Keep-out 2.00
- **s100m200k200** = Square Land 1.00 with Solder Mask 2.00 with Keep-out 2.00

## Example of Proportional Plated Through-hole Pad Stack

- **c150h100** = 1.50 circular pad with 1.00 hole with 1.50 solder mask with 1.50 plane clearance with 1.50 assembly outline with Thermal Relief w/4 spokes 0.40 width with ID 1.50 and OD 1.80

## Example of Proportional Non-plated Through-hole Pad Stack

- **c100hn150** = 1.00 circular pad with 1.50 hole “non-plated” with 1.50 solder mask with 2.35 plane clearance with 2.10 keep-out

# 14.0 – ODA Pad Stack Naming Convention

The pad stack consists of combinations of letters and numbers that represent shape, or dimensions of lands on different layers of printed boards or documentation. The name of the pad stack needs to represent all the various combinations. This pad stack naming convention was created by Optimum Design Associates.

The first part of the pad stack convention consists of a land shape. There are six basic land shape identifiers. Note: All alphabetical characters are “UPPER CASE”. All numeric values are represented in Micrometer units.

## Basic Land Shape Letters

- C = Circular
- S = Square
- R = Rectangle
- B = Oblong
- G = Octagonal
- F = Finger D Shape
- SR = SMD Rectangle
- SRCR = Surface Rounded Corner Rectangle
- THP = Through Hole Plated
- THN = Through Hole Non-plated
- SU = User Defined Contour
- DC = Donut Circular outside diameter
- IDC = Inside Donut Circular
- TC = Thermal Circular
- TS = Thermal Square
- TB = Thermal Oblong
- TR = Thermal Rectangle
- MHP = Mounting Hole Plated
- MHN = Mounting Hole Non-Plated
- V = Via
- FID = Fiducial

**Illegal characters:**
" " , ; : / \ [ ] ( ) . { } * & % # $ ! @ ^ =

## Name Structure Order

**SR2000X1000**
Surface Mount Rectangle 2.000 X 1.000

**THP090C1500**
Through-hole Plated 0.90 Hole, Circular 1.500 Pad

**SRCR2430X2370X0050**
Surface Rounded Corner Rectangle 2.430 long X 2.370 short X 0.050 corner radius

**Separator Convention**
‘X’ is used to separate dimensions within a given shape, and ‘_’ is used to separate the different aspects of the naming convention.

**Example:** SR0640X0630_SM0660X0650 (Solder Mask callout appended when SM deviates from the standard overage of .05 on each side / .1 overall expansion. In this example, .01 on each side / .02 overall expansion is used.)

## Dimension Order

Any time the pad is longer on one side than the other, the longest edge is presented first in the pad stack naming convention.

## Solder Mask Modifiers

- _NSM = None
- _SSM = Both Sides
- _TSM = Top Side Only
- _BSM = Bottom Side Only
- _STM = Specified Top
- _SBM = Specified Bottom
- _TNTT = Tented Top
- _TNTB = Tented Bottom
- _CAPT = Via Cap Top
- _CAPB = Via Cap Bottom

## Solder Paste Modifiers

- _NSP = No Solder Paste
- _SSP = Specified Size Paste
- _TSP = Top Specified Paste
- _BSP = Bottom Specified Paste

## Layer and Size Modifiers

- _INP = Inner Layer Pad Size
- _BTP = Opposite/Bottom Side Pad
- _BOT = Bottom Surface Mount

## Thermal and Plane Modifiers

- Thermal Spoke Count = 4 Ties at 45° is default
- TC or TS or TB or TR + D (Hole) + A (Annular) G (Gap) T (Tie) – **TCD125A0120G0100T0120**
- BTH = Buried Thermal
- THRM = Via with Thermal Relief

## Miscellaneous Modifiers

- _OFF = Offset
- _OBS = Keep-out/Obstruct
- _N = Non-Plated Hole
- _TOL (+tol)X(-tol) – TOL0105X00075
- _VT = Via Tolerance
- _PCH = Punched Hole
- _PFIT = Press Fit
- _UV = Microvia
- _BWT = Bottom Wave Tech

## Chamfered and Radius Corner Pad Stacks

Chamfered corner pad stacks are named as custom pad stacks (SU_ prefix) or are to be drawn at the CAD tool footprint level rather than be included in the pad stack.

Radius cornered pads fall under B obrounds (4 corners) or F fingers (2 corners). Rounded corner rectangles (where the corner radius does not form a full obround or finger) use the SRCR prefix: SRCR + long side X short side X corner radius value (e.g., SRCR2430X2370X0050). Any other non-standard corner configuration would fall under SU custom pad/pad stack naming.

### User Defined / Custom Pad Stacks

Named specifically since they won't be used generically and are seen as being used 1 to 1 with a part number or package.

- SU_MFR_MPN(OR PACKAGE ID)_#
- SU = custom pad stack
- MFR = Manufacturer
- MPN or PACKAGE ID = Manufacturer Part number or Manufacturer Package ID

# = arbitrary character if more than one custom pad is on the device either 1, 2, 3 etc. or L and R for left and right

**Alternate SU format**
SU_ManufacturerPrefix_CaseCode_#

**Example:**
SU_TI_RRX0029B_1 (Texas Instruments, RRX0029B case code, pad variant 1)

## Default Values

- Solder Mask Size – 0.100 larger than pad
- Paste Mask Size – 1:1 scale of pad size
- Inner Layer Shape – Round internal pads for Square through-hole pad
- Thermal Ties – 4 ties at 45 degrees
- Via Thermals – Buried thermal (no relief)
- Drill Tolerance – ± 0.075 mm (holes ≤ 2.50 mm) or ± 0.10 mm (holes > 2.50 mm)
- Via Drill Tolerance – + 0.075 mm / - hole size

## Individual Pad and Hole Naming Convention

In addition to the pad stack name, the individual pads and holes within a pad stack follow their own naming conventions. These names are derived from the parent pad stack name and describe the specific layer-level objects.

## SMD Pad Naming

For surface mount pads, the individual pad name is derived from the pad stack name by removing the leading "S" prefix. The pad dimensions in the name remain identical to the pad stack.

**Convention:** Remove the "S" prefix from the pad stack name. The resulting name is assigned to the copper pad on most layers.

**Solder Mask Pad:** When solder mask uses the default expansion (0.05 mm per side / 0.10 mm overall), the mask pad name reflects the expanded dimensions using the same format.

**Example:** Pad stack SR0860X0250 → Copper pad name is R0860x0250 (assigned to most layers), Solder mask pad name is R0960x0350 (reflects the 0.05 mm per side expansion).

## Through-Hole and Mounting Hole Naming

Holes within through-hole and mounting hole pad stacks are named to describe the hole shape, diameter, and plating status.

**Convention:** The hole name follows the format: Shape + Diameter + Plating Suffix.

**Shape:** "Rnd" for round holes.

**Diameter:** Expressed in millimeters (e.g., 0.40 for a 0.40 mm hole).

**Plating Suffix:** "P" for plated holes, "N" for non-plated holes.

**Example:** Rnd 0.40P = Round, 0.40 mm diameter, plated hole.

**Example:** Rnd 3.20N = Round, 3.20 mm diameter, non-plated hole.

**Hole Tolerance Suffix**

**Default tolerance:** ±0.075 mm for holes up to 2.50 mm, and ±0.10 mm for holes larger than 2.50 mm. When the default tolerance applies, no suffix is appended to the hole name.

**Non-default tolerance:** When a tolerance other than the default is required, a _TOL suffix is appended to the hole name. The suffix value is expressed in micrometers representing the ± tolerance.

**Example:** Rnd 0.40P_TOL0050 = Round, 0.40 mm, Plated, with ±0.05 mm tolerance (instead of the default ±0.075 mm).

**Example:** Rnd 3.00P_TOL0150 = Round, 3.00 mm, Plated, with ±0.15 mm tolerance (instead of the default ±0.10 mm).

**Pad Stack Name Examples**

## Surface Mount Pads

- Rectangle SMD 2.00 x 1.00 – SR2000X1000
- Oblong SMD 3.00 x 1.50 – SB3000X1500
- Square SMD 3.50 – SS3500
- Circular SMD 1.00 – SC1000
- Rounded Corner Rectangle SMD 2.430 x 2.370, 0.050 corner radius – SRCR2430X2370X0050
- Rectangle with custom Solder Mask – SR3000X1500_SSM3300X1800
- Rectangle with custom Solder Paste – SR3000X1500_SSP2700X1200
- Rectangle with Offset Origin – SR3000X1500_OFF0500
- Custom pad Texas Instruments RDM package left side – SU_TI_RDM_L

## Through-hole Pads

- 0.90 Plated hole, Circular 1.50 pad – THP090C1500
- 0.90 Plated hole, Square 1.50 pad – THP090S1500
- TH with Inner layer pad different size – THP090C1500_INP1400
- TH with Opposite side pad different size – THP090C1500_BTP1700
- 0.90 non-plated hole, Circle 1.50 pad – THN090C1500
- Plated Oblong Slot 3.00 x 1.00, pad 4.00 x 2.00 – THP300X100B4000X2000

**Individual Pad and Hole Name Examples**

- SR0860X0250 → Copper pad: R0860x0250, Solder mask pad: R0960x0350
- SS3500 → Copper pad: S3500, Solder mask pad: S3600
- THP090C1500 → Hole: Rnd 0.90P (default tolerance ±0.075 mm, no suffix)
- THP040C1000 → Hole: Rnd 0.40P_TOL0050 (non-default tolerance of ±0.050 mm)
- THN320C5000 → Hole: Rnd 3.20N (non-plated, default tolerance ±0.10 mm)
- MHP400C7000 → Hole: Rnd 4.00P (default tolerance ±0.10 mm)

**Vias**

- Standard via 0.50/0.25 – V025C0500
- Square via 0.50/0.25 – V025S0500
- Via with opposite size – V025C0500_BTP0700
- Blind via L1-L3 – V015C0300 (layer in tool)
- Via with thermal relief – V025C0500_THRM

**Mounting Holes**

- Plated MH 4.00 hole, 7.00 pad – MHP400C7000
- Non-Plated MH 4.00 hole – MHN400
- MH w/ inner layer & mask – MHP400C7000_INP5200_SSM7200

**Fiducials**

- Circular 1.00, mask 2.00, KO – FID_CELL_1000
- Global fiducial – FID_GLOBAL

## ODA Footprint Naming Convention

Footprint names follow IPC-7351 conventions where applicable. The material condition suffixes L, N, and M are used when the IPC nominal land pattern is selected.

## IPC Nominal Land Pattern (L, N, M suffixes)

When the IPC nominal land pattern is used, the standard IPC material condition suffixes apply:

- L = Least material condition (most solder fillet)
- N = Nominal material condition
- M = Most material condition (least solder fillet)

**Example:** SOT23-5P95_290X280X145L45X40N

## IPC Standard Package with Manufacturer-Recommended Footprint (Q suffix)

If the package type is an IPC standard one but the manufacturer-recommended footprint is chosen instead, the Q material condition suffix is used per our standard in place of L, N, or M, followed by the manufacturer prefix and the case code.

**Example:** SOT23-5P95_290X280X145L45X40Q_TI_DBV0005A

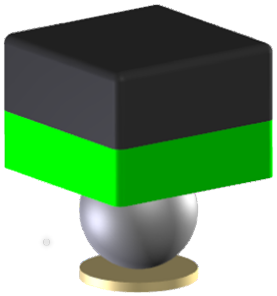
## Non-IPC Standard Package or RF Component (Manufacturer Prefix + Case Code)

If the package type is not an IPC standard one, or if it is an RF component, the manufacturer-recommended footprint is used and named with the manufacturer prefix and case code directly.

**Example:** TI_RRX0029B

# 15.0 – Terminal Lead Forms

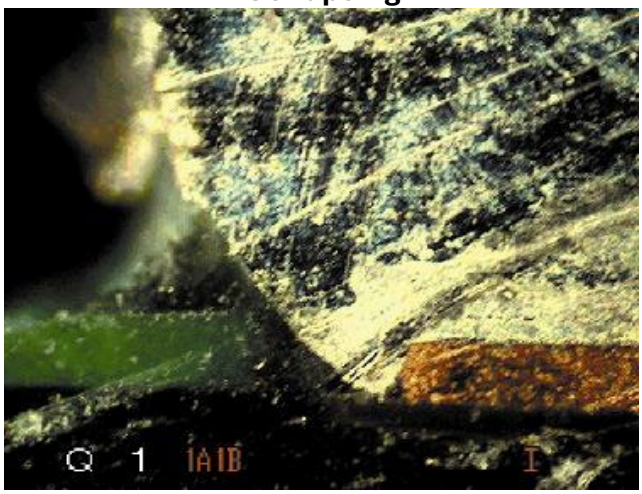
## Ball Grid Array



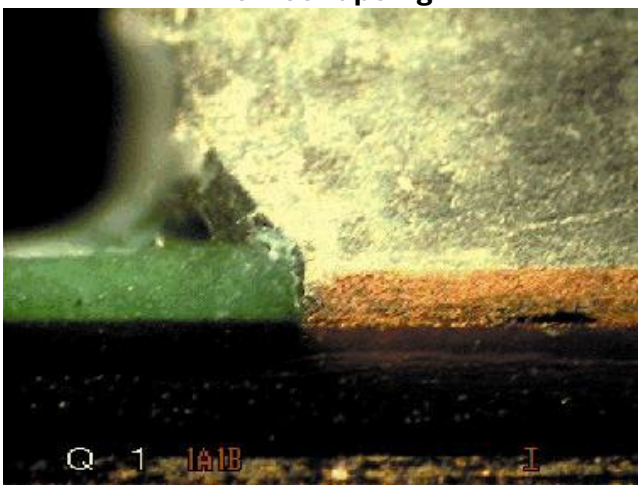
A surface mount integrated circuit packaging type that utilizes a matrix of small solder spheres (solder balls) on the underside of the component to establish external electrical connections to a printed circuit board (PCB). By replacing traditional perimeter-only leads or pins with a full-surface area array, BGAs provide drastically higher interconnect density. This configuration optimizes electrical performance through shorter internal trace paths, dramatically reducing parasitic inductance and impedance in high-speed applications.

There are Collapsing and Non-collapsing BGA balls.

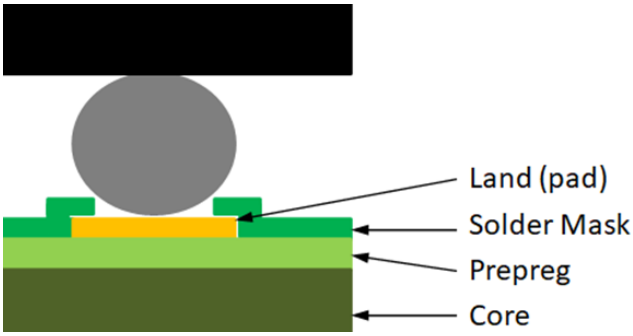
## Collapsing



## Non-collapsing

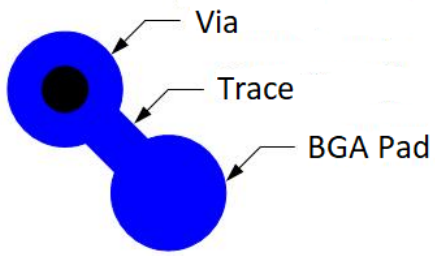


There is also a Solder Mask Defined BGA that has solder mask over the pad edges. The annular ring of the solder mask on pad is typically 0.05 mm. This technology is primarily used to secure the PCB pad to the PCB prepreg in handheld devices like cell phones. During drop tests, the solder joint between the BGA ball and the pad remains intact, but the pad could separate from the prepreg. Solder mask and prepreg are both epoxy resin (glue). The solder mask will help secure the pad to the prepreg to prevent the pad separating from the prepreg. This solder mask defined concept is primarily used on BGA pin pitches of 0.65 mm and lower, where the non-collapsing pad size is larger than the BGA ball diameter.



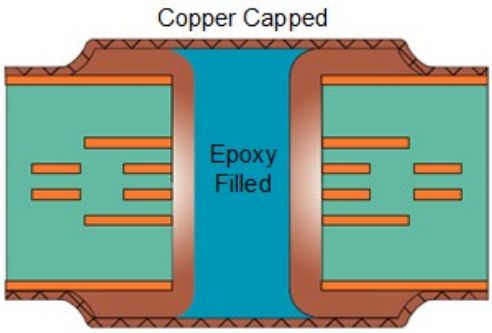

The primary reason for making the BGA pad size larger than the ball diameter is to accommodate via-in-pad technology because fine pitch BGAs cannot use the typical Dog-bone via fanout solution.

**Dog-bone via fanout:**

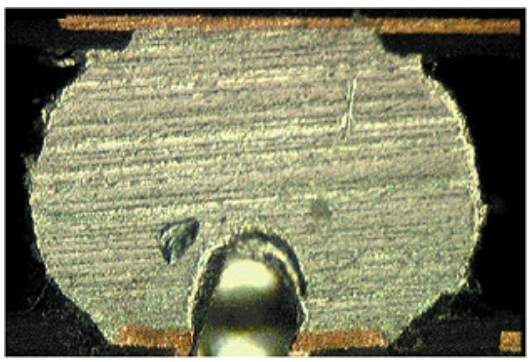



When creating dog bone fanouts for BGAs, the escape trace should be kept as wide and as short as possible. Generally, the trace is a wide as the ball width. A wider trace reduces series inductance, which is critical because the fanout forms part of the high frequency return path loop between the BGA ball, via, and internal plane. Narrow traces behave like inductors at RF, increasing impedance, degrading signal rise time, and injecting noise into adjacent balls.

**Via-in-Pad technology** is a technique used in PCB design where the via is placed directly in the pad. This approach is commonly used in high-density interconnect (HDI) designs, especially for fine pitch BGAs.

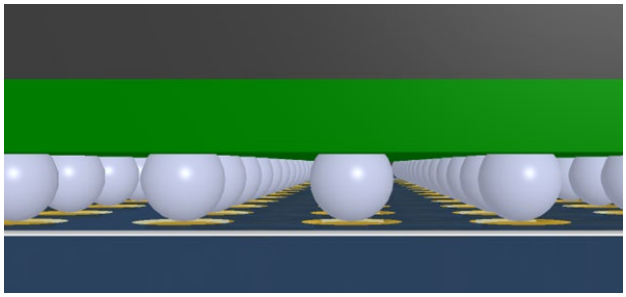



The via-in-pad (VIP) requires a separate fabrication process that includes plating, plugging and capping the hole and planarizing the capped pad to create a flat surface with no dimples. Capped pads with dimples create trapped air under the paste mask. When the PCB goes through the reflow oven, the trapped air in the pad dimple gets super-heated and blows through the solder and into the BGA ball causing a void.



Most of the time the via-in-pad is a microvia that goes from the top layer to the first signal layer. Then buried vias connect to all the other inner layers. All BGA GND connections use microvias to Layer 2. However, PCB fabrication can now drill a hole with a 10:1 aspect ratio. A 1.57 mm thick PCB can support a via hole size of 0.15 mm. But the pad size must be 0.35 to support a 0.10 mm annular ring. This solution is good for 0.40 – 0.65 mm pitch BGAs.

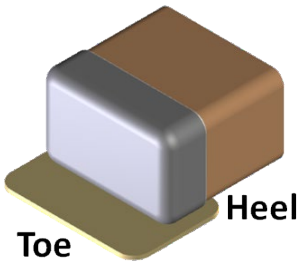
The free Footprint Calculator and the Footprint Expert use these tables for BGA footprint calculations. The Footprint Expert also creates high-quality BGA footprints and 3D STEP models directly from the package dimensions.



**BGA Ball Materials:**
The BGA ball may consist of a variety of metal alloys. Some of these include balls with some lead content such as 37Pb63Sn, 90Pb10Sn, 95Pb5Sn, while others do not contain lead such as Sn96.5Ag3.0Cu0.5, Sn96.5Ag3.5, Sn-9Zn-0.003Al. It is a good recommendation to use the same alloy, in a paste form, to attach the BGA balls to the mounting substrate; however, some of the balls that do not collapse require a paste that is more conducive to reflow temperatures.

Lead-free balls have a combination of tin, silver and copper. This is the replacement for the tin/lead ball. BGAs are usually assembled using the standard reflow solder processes.

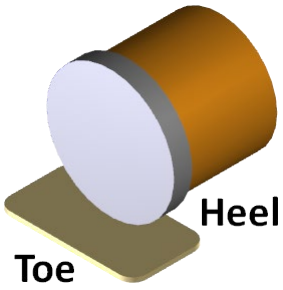
## Rectangular or Square End Cap




Metallized end bands or chip terminations) are the metal contact structures covering the opposing ends of passive surface mount electronic chip components. Unlike integrated circuits that use external pins, these terminal leads envelop the outer structural corners of the device to facilitate structural mounting and complete an electrical circuit. They are the standard terminal configuration for

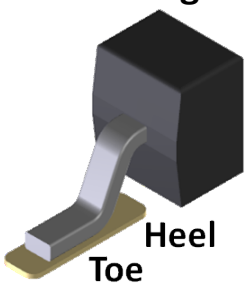
surface mount capacitors, resistors, thermistors, varistors, chokes, ferrite beads, antennas, crystals, diodes, filters, fuses, LEDs and inductors. This is the most popular lead form as chip components are usually 80% of the components on a PCB layout.

## Cylindrical End Cap




A cap-shaped, round metal contact covering the opposing ends of a cylindrical component body. Rather than using protruding wires or flat rectangular bands, MELF components utilize these flush, circular metal barrels as their electrical and mechanical mounting interfaces. This terminal style is widely utilized for high-reliability surface mount resistors, diodes, and Zener regulators in automotive, industrial, and aerospace electronics.

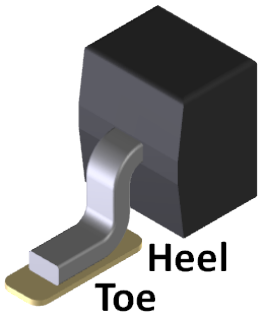
## Gullwing



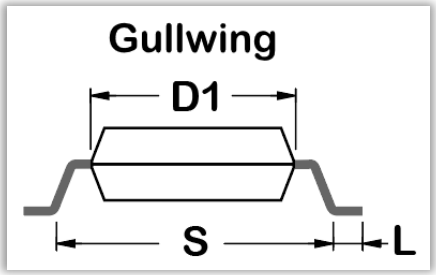

An outward-bent surface mount technology (SMT) lead shape that resembles a seagull's wing in flight. The metal leads extend horizontally from the sides of an integrated circuit (IC) package, bend vertically downward toward the circuit board, and then bend outward again to create a flat mounting foot. This flat foot provides the primary electrical and mechanical contact surface for soldering onto a printed circuit board (PCB) land pad.

Gull wing leads are the dominant terminal style for highly utilized IC packages such as Small Outline Integrated Circuit (SOIC), Thin Small Outline Package (SOP), Quad Flat Package (QFP), Small Outline Transistor (SOT), Ceramic Flat Pack (CFP), Ceramic Quad Flat Pack (CQFP), Small Outline Diode (SOD) and DPAK.

## Outward L Lead

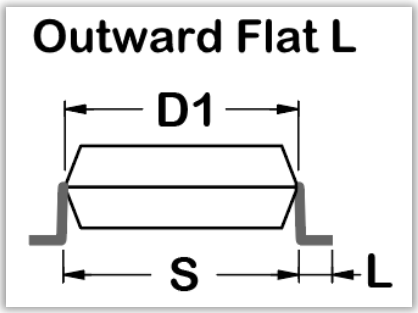



Certain small Surface Mount components, such as some SOD's and SOTs for example, with terminal leads that can be in the form of either *Gullwing* or *Outward flat 'L'* depending on their dimensions. It's important to distinguish between the two to assign the correct protrusion goals (toe, heel and side) to obtain the most reliable footprint mounting. This is how the PCBL Footprint Expert does it.




**Gullwing** terminals are generally for parts with relatively larger terminals and provide more heel fillet.

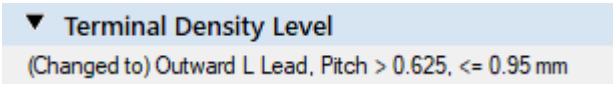
*Gullwing* goals should be applied when:
S min > D1 max **OR** (L max – L min) >= 0 .5mm



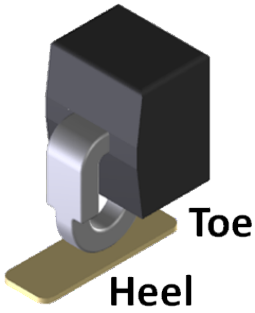

**Outward Flat L** terminals are generally for smaller parts and do not provide as much heel fillet.

*Outward Flat L* goals should be applied when:
S min <= D1 max **AND** (L max – L min) < 0.50 mm

When a *Gullwing* change to *Outward L* occurs, this message will be displayed:

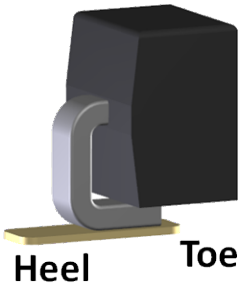



## J-Lead



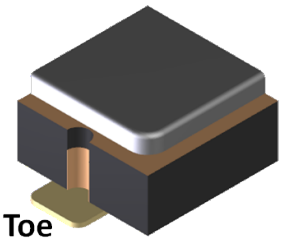

A specialized surface mount technology (SMT) component lead form that curves downward and tightly rolls underneath the package body in the shape of the letter "J". This configuration stands in contrast to Gullwing leads which extend outward. J-leads are widely used on Plastic Leaded Chip Carriers (PLCCs), memory modules, and tactile switches to reduce board footprint while maximizing mechanical compliance.

## Inward L Lead



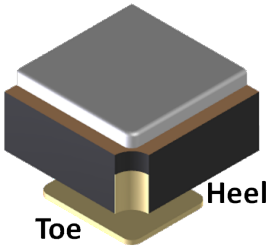

An Inward L-Lead form is a surface mount technology (SMT) component lead configuration where each terminal extends from the package body, bends downward at a right angle, and then bends sharply inward toward the center of the component body. This creates a low-profile, right-angle connection footprint that sits entirely underneath the perimeter of the device. It is primarily utilized on Small Outline L-Bend (SOL) packages and high-density ribbon assemblies to maximize available circuit board area.

## Side Concave



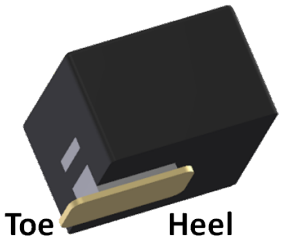

A specialized surface mount technology (SMT) terminal design where the conductive contact pad curves inward toward the body of the component, forming a scalloped indentation or semicircular castellation along its edge. This design is primarily used on dense passive components like side-concave chip resistor arrays, multi-layered ceramic capacitor (MLCC) arrays, and edge-mounted castellated sub-modules (such as Wi-Fi/Bluetooth breakout boards)

## Corner Concave




A surface mount component termination style where the conductive pads form scalloped, crescent-shaped vertical castellations directly on the outside corners of the device body. This configuration is most prominently featured on surface mount quartz crystal oscillators, clock generators, and specialized square filter modules.

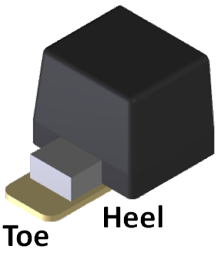
## Flat No-Lead Side




A PCB Flat No-Lead Side terminal lead (commonly categorized under flat, no-lead side terminations) refers to the perimeter signal pads found on Bottom Termination Components (BTCs). These are used on Quad Flat No-Lead (QFN) and Dual Flat No-Lead (DFN) packages.

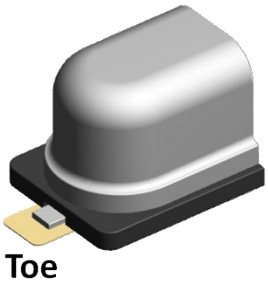
The contacts do not project from the package sides; instead, they exist as flat metalized lands on the bottom face that terminate flush with the outer cut edge of the component wall.

## Flat Lead



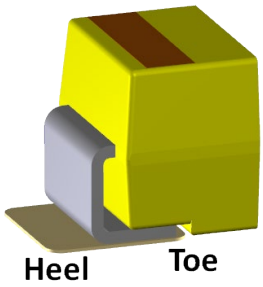

A surface mount or through-hole termination style where the component pins consist of flat, unbent, thin metal strips extending horizontally or vertically from the package body. Unlike round wire leads or pre-formed Gullwing leads, flat leads are completely linear and planar. They are primarily utilized on high-current surface mount inductors, flat-pack aerospace ICs, current-sense resistors, and planar transformers.

## Under Body Outward L




A lead variant where the pins exit from the bottom or lower edge of the component casing, bend outward, but remain entirely hidden beneath the perimeter outline of the component package. Unlike standard Gullwing leads which extend well past the sides of a chip, or Inward L-Leads which hook back inward beneath the component frame, the Under-Body Outward L lead steps outward away from the package center but terminates *before* exiting the package bounds. It is most frequently found on Aluminum Electrolytic Capacitors, Crystal Oscillators, heavy shielded power inductors, and specialized SOT sub-packages.

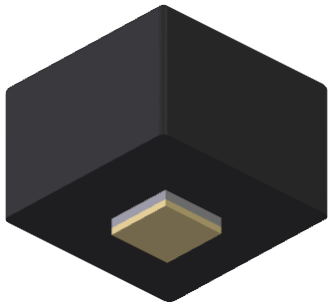
## Inward Flat Ribbon L




A specialized surface mount technology (SMT) lead configuration that combines the low-inductance, flat cross-section of a flat-ribbon lead with the space-saving geometry of an inward L-bend.

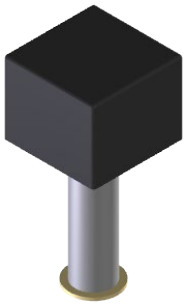
Instead of extending outward from the component body like a standard flat ribbon lead, the lead extends downward and then bends sharply at a right angle toward the center of the component body. This ensures the entire flat contact foot is tucked cleanly beneath the device perimeter. Used for Capacitors, Inductors, Diodes, LEDs, Chokes, Ferrite Beads, and Filters.

## Land Grid Array/Bottom Only



A surface mount connection interface where the component features a grid of flat, coplanar metal pads on its bottom surface instead of protruding pins or solder balls. Electrical and mechanical connection to the PCB is established via a matching pattern of landing pads and an ultra-thin layer of solder paste, or through a mechanical socket. This architecture is widely used for high-performance processors, complex field-programmable gate arrays (FPGAs), wireless modules, and high-density sensors.

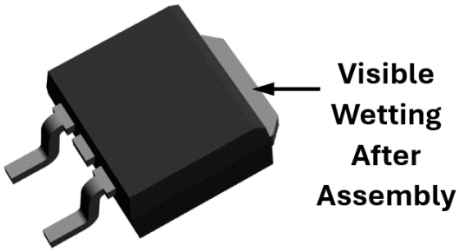
## Column Grid Array



An advanced high-density surface mount packaging interface. Instead of utilizing spherical balls like a standard Ball Grid Array (BGA), a CGA utilizes an array of tall, cylindrical high-temperature solder columns or copper-reinforced posts that stand vertically on the underside of the component package.

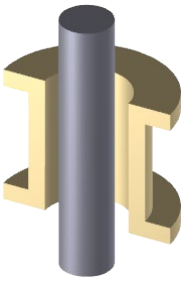
This termination style is highly specialized and explicitly preferred for large-body integrated circuits (such as space-grade FPGAs, processors, and telemetry modules) operating in harsh environments where extreme thermal fluctuations and severe mechanical vibration are constant.

## Flat Lug Lead (DPAK Tab)




A large, heat-dissipating backside drain tab of a DPAK (TO-252) surface-mount package into a dedicated flat, surface-mounting contact terminal. It serves as the primary path for drawing destructive heat away from the silicon die and distributes it directly into the copper planes of the printed circuit board. In standard power MOSFETs, this extended tab functions as the high-current electrical connection for the Drain terminal. Avoid applying a 1:1 ratio of solder paste to the flat lug pad area. Industry guidelines from manufacturers like onsemi recommend a windowpane or checkerboard stencil pattern covering roughly 60% of the tab area. This prevents component floating, misalignment, or "tombstoning" from excess solder. The Nominal Toe value is 0.35 mm and must have visible wetting after assembly. The Side and Heel values are very small and set to 0.03 to maintain alignment and prevent skewing. However, some voltage regulator DPAK devices produce additional heat and the manufacturer recommended pattern for the thermal pad size should be taken into consideration. To maximize heat transfer from the flat lug lead, stitch multiple thermal vias into the pad connecting to inner or bottom-layer ground/power planes. Due to the massive heat-sinking nature of the extended tab, hand-soldering requires a large thermal mass iron, a pre-heating hot plate, or a secondary heating source to ensure proper solder flow under the heel of the component.

## Through-Hole



Through-hole leads rely on mechanical insertion through the substrate. Pre-forming the leads is a critical manufacturing step designed to establish a consistent component standoff height, provide strain relief, and mechanically lock the component to the board prior to wave or selective soldering.

# 16.0 – Pad Shapes

## 16.1 – Surface Mount

**Oblong**
Recommended by IPC-7351

**D-Shape**
Recommended by some component manufacturers

**Rectangle**
Recommended by most component manufacturers

**Square**
Used on Land Grid Arrays (LGA)

**Rounded Rectangle**
Recommended by assembly shops for better stencil release
The default corner radius is 0.10 mm

**Round**
Used on Grid Arrays (BGA. CGA and LGA)

## 16.2 – Through-hole

**Square**
Used on Pin 1 for Polarity on Diodes and Polarized Capacitors

**Rounded Square**
Used on Pin 1 for Polarity on Diodes and Polarized Capacitors

**Round**
Used on all through-hole parts

## 16.3 – FP Designer Surface Mount

FP designer includes all calculator pad shapes. These are the custom pad stacks available in FP Designer.

Rectangle and square pad shapes can be chamfered in 2 corners on the Top, Bottom, Left and Right sides.

**Top Chamfer**

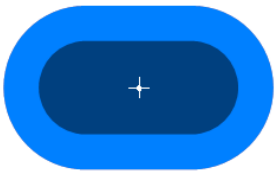
Chamfered on one Corner in Upper Left, Lower Left, Upper Left, Upper Right.

**Upper Left**

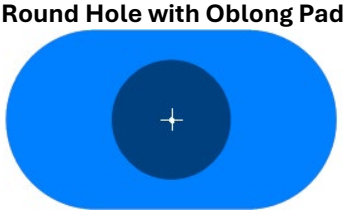
**Chamfer Lower Left with Radius corners**

## 16.4 – FP Designer Through-hole

**Slotted Hole**

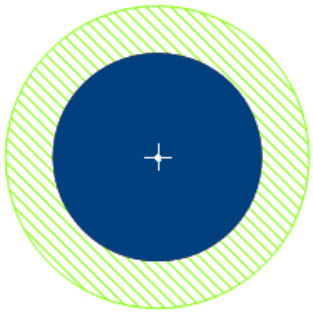


**Round Hole with Oblong Pad**



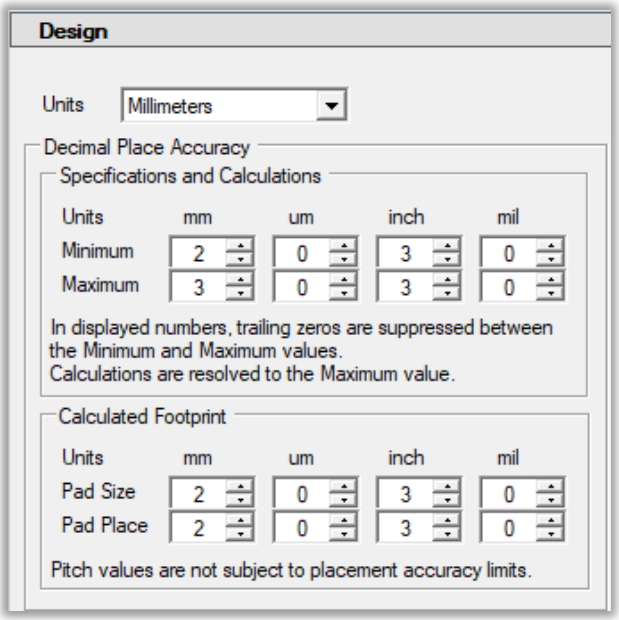
**Offset Slotted Hole**

**Non-Plated Hole**



# 17.0 – Design Units

**Design Units User Interface**




There are 4 options (millimeter, micrometer, inch, mil) for units, but millimeter is the most popular today because most package dimensions in manufacturer datasheets are displayed in millimeter units.

**Decimal Place Accuracy > Minimum / Maximum**
Most PCB Library Parts are created in millimeter units to match the current package datasheet, but everyone is in a different environment. The new "Units" allows you to set the Minimum and Maximum rounding values.

By setting the Minimum and Maximum values, you establish the program rounding values.

Example 1: using 2 place Minimum accuracy, entering a 0.8 value, will display as 0.80. The program will automatically add a trailing zero to round the value 2 place minimal accuracy.

Example 2: using 2 place Maximum accuracy, all values will be rounded up to the nearest 0.01. Entering a 0.025 value would display as 0.03.

The program default settings are Minimum 2 and Maximum 3. Because the minimum is 2, the program will automatically remove all training zero's past 2 places. And the maximum setting of 3 will only round up values less than one micrometer.

Example 3: using a 3 place Maximum accuracy, a value of 0.3255 will be rounded up to 0.326

Example 4: using a 2 place Minimum accuracy, a value of 0.29 will be rounded up to 0.30

- 4 units = 0.0001
- 3 units = 0.001
- 2 units = 0.01
- 1 unit = 0.1

The most important thing is that both the minimum and maximum options go up to 6 places. This accuracy is intended to increase the rounding accuracy when converting between Metric and Imperial units. It is not recommended that users select 6/6 as their min/max because this will affect the Physical Description that is auto generated by Footprint Expert in the FPX file. Having every value 6 places to the right of the decimal point would also affect every component family calculator, as every value will be rounded and displayed with 6-point accuracy. A simple value of 0.01 would display as 0.010000 and the Physical Description would be the same.

# 18.0 – FPX File Definition

The FPX file library is a collection of package dimensions for standard parts and manufacturers recommend patterns for non-standard parts. Standard part footprints are created in the calculator using one of the 144 surface mount or through-hole templates. Non-standard parts are created using the FP Designer module in Footprint Expert.

All connectors are non-standard parts except headers that have a symmetrical pad pattern with one pad stack and the pins are evenly placed using the same X/Y grid system. Any semiconductor that requires more than one pad stack length or width is a non-standard package. Any discrete component that its terminal lead form is not listed in the surface mount standard terminal leads is considered a non-standard package.

The Calculators save this information in the FPX file library:

1. Package Dimensions
2. 3D STEP Color
3. Manually inserted Drafting Symbols
4. Manually inserted Keepout
5. Manufacturer Recommended Pattern
6. Manually Updated Pin Names or Reordered Pins

All other footprint features are generated in Tools > Options. When you open a FPX file calculator part, the package dimensions will auto-populate the package dimensions in the correct cells. The resulting footprint is derived by combining the package dimensions with the Terminal Solder Joint Goal Settings for that component family and the Drafting Rule Settings for silkscreen, assembly, courtyard, component, terminal and origin outlines. The package and terminal tolerances also play a role in the pad stack calculation.

You can create multiple Option files with different rule settings and use the same FPX file to create multiple libraries. Set up Options to solder mask define pad stacks for Flex circuits. Or set up rules with larger solder joint goals for Wave Solder. Or create an Option file with rules from an assembly shop or rules for a specific customer. Use the same FPX file to create multiple libraries for different applications.

For non-standard FP Designer parts, a lot more data is saved in the FPX file. FP Designer footprint data that is saved in the FPX file include:

1. 3 Package dimensions
2. Pad Stack Data
3. Courtyard Excess
4. Manually inserted Drafting Symbols
5. Automatic Assembly Polarity Location
6. Manually inserted Keepout
7. Footprint Rotation
8. Physical Description
9. Manufacturer Name
10. Case Code
11. Part Number
12. Pin Names
13. Footprint Origin Location
14. Footprint Name
15. 3D Color

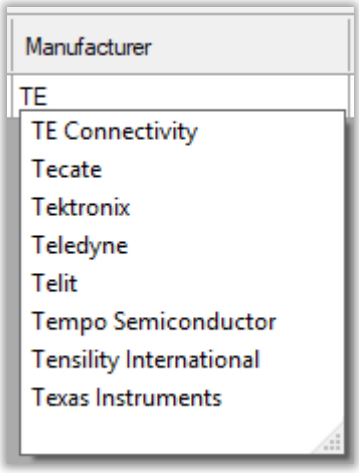
The FPX file comes with these column headers, but you can add additional columns:

1. Footprint Name
2. Physical Description
3. Case Code
4. Manufacturer
5. Part Number
6. Logical Description
7. Mounting Type
8. Datasheet
9. Part Status
10. Footprint Date
11. Comments

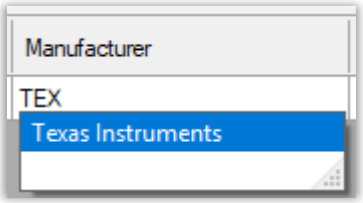
The FPX file has built in features that help automate and organize library data. When you select a Calculator component family and enter the package dimensions and Save to FPX Library, Footprint Expert autogenerates the Footprint Name, Physical Description, Mounting Type, Part Status and Footprint Date. The Manufacturer Names are embedded into the program. When the Manufacturer cell is selected, just enter the first couple letters of the Manufacturer Name and a list of Manufacturers appear in a dropdown menu selection.

By typing a 'T' in the Manufacturer cell, every manufacturer name that begins with 'T' will appear in the dropdown menu.

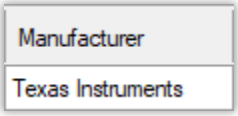

Type 'TE' and the list will only include manufacturer names that include 'TE'.




Type 'TEX' and the list will only include manufacturer names that include 'TEX'. Texas Instruments is the only manufacturer that begins with TEX. Select Texas Instruments and it will auto-populate the Manufacturer cell.

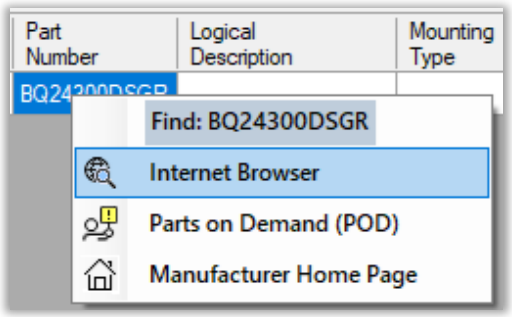



This will ensure that all the spelling of every manufacturer is consistent.




The Case Code and Part Number must be manually entered or copy/paste from a datasheet.

Once the full Part Number is populated, you can Right Mouse Click that cell and a dropdown menu will appear with these options:




When '**Internet Browser**' is selected, the default web browser will display all the websites that support that Part Number.

When '**Parts on Demand (POD)**' is selected, the default browser will open www.pcblibraries.com/POD allowing you to download that part into your /downloads folder. Then you can import the FPX file into your Master Library and create the footprint out to your CAD tool.

When '**Manufacturer Home Page**' is selected, the main page to that Manufacturer will open in your default browser., You can copy/paste the part number into the search box to locate the datasheet.

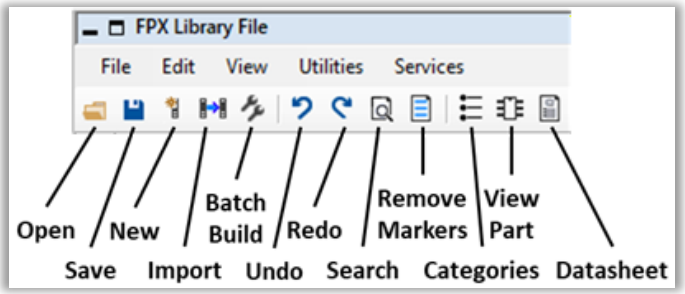
Note: The Part Number search requires the Manufacturer Name cell to be populated.

The same feature is available if you have the correct Case Code cell entered.

The '**Datasheet**' cell can be https:// or a network drive path to a PDF datasheet.

The '**Mounting Type**' cell can be auto populated by entering a **S** for Surface Mount or **T** for Through-hole or **M** for Mixed Technology.

Here are the control features for the Library Editor.




- Open an existing FPX file library
- Save the current FPX file (this icon will turn gray when the file is saved)
- Create a New FPX file
- Import an FPX file into an existing FPX file
- Batch Build a selection of parts to CAD tool
- Unlimited Undo
- Unlimited Redo
- Search for text in the FPX library
- Remove all highlighted Markers
- Show a list of component family Categories
- View the selected footprint
- Open the Datasheet

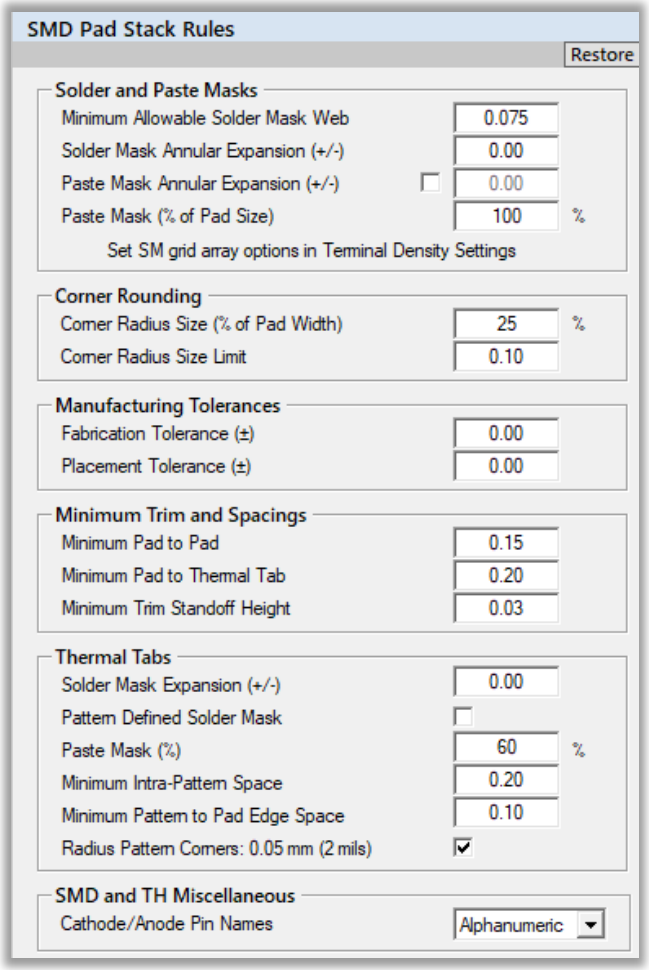
Delete a Row by selecting the gray button to the left of the Footprint Name and Right Mouse Click and select 'Delete Row'.

Add a new blank row by Right Mouse Click and select 'New – Row' or 'New – Rows'.

Add a new column by Right Mouse Click and select 'New – Column'. Create as many columns as you need.

# 19.0 – SMD Pad Stack Rules

Pad Stack Rules will globally define the rules for every footprint created in the Surface Mount Calculators. These rules are not used for custom FP Designer footprints because the user manually defines every pad stack in custom parts. Custom footprints always use the component manufacturer recommended pattern and pad sizes because there are no standard recommendations or guidelines for unique packages and their related footprint patterns. The default values are best known practice, but users can edit any value for their PCB library requirements.




## 19.1 – Solder and Paste Masks

**Solder Mask Note:**
Solder mask is an epoxy coating that protects the circuit from corrosion and electrical shorts. It also provides electrical insulation that allows higher voltage traces to be placed nearer to each other.

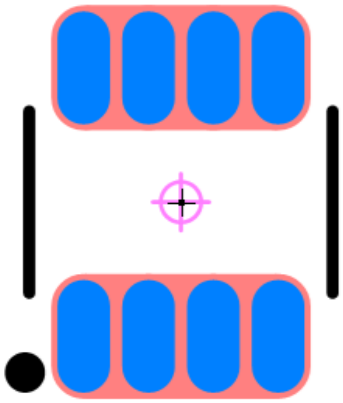
Most importantly, the solder mask keeps the solder on the pads, as opposed to flowing onto traces, planes, or empty board space. This reduces the likelihood that solder will form bridges (unintended connections) from one element to another. Solder masks are critical for wave soldering, which is a mass production technique. Solder masks also make hand soldering faster, easier, and more accurate.

**a. Minimum Allowable Solder Mask Web – 0.075** or **0.10**
This rule is for PCB fabrication. The solder mask stencil must have a minimum 0.075 mm between pads. Anything less than that is not manufacturable. When the solder mask web violates the minimum value, Footprint Expert will automatically gang the solder mask into a solid block. If you provide Gerber data with a solder mask web less than 0.075 mm to fabrication, they will automatically gang mask the row of pads for you, and not tell you. If you provide 1:1 scale solder mask to fabrication, they will swell the mask to meet their fabrication tolerance for their solder mask application. Fabrication CAM tools will alert the operator of all solder mask webs less than 0.075 and the operator will gang mask all solder mask areas that violate the minimum solder mask web.

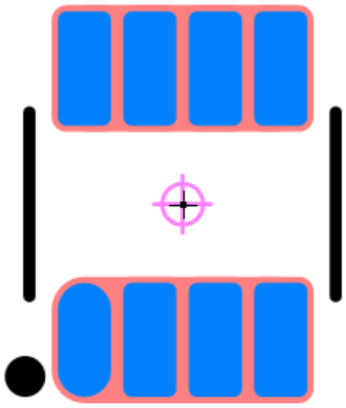
**b. Solder Mask Annular Ring Expansion – typically between 0.05 – 0.075**
Some PCB designers use a solder mask expansion between 0.05 – 0.075 because they use that as a visual for placing reference designators on a final part placement. Silkscreen Legend Ink should not be in an exposed solder mask area. If you place silkscreen legend in a solder mask free area in your PCB layout, the fabrication process will automatically trim the silkscreen legend away from the free solder mask area. But many PCB designers leave the solder mask 1:1 scale of the pad and allow the PCB fabrication shop to automatically swell all solder mask features to meet their solder mask registration tolerance.

**c. Paste Mask (% of Pad Size) – 100%**
Normally, paste mask on pads is 1:1 scale but this option allows the user to increase or reduce the amount of Paste Mask on a pad.

**d. Gang Solder Mask**
When the Solder Mask Annular Expansion rule is violated, Footprint Expert will automatically Gang Mask the entire row. This image illustrates an Oblong pad shape Gang Mask



This image illustrates a Rounded Rectangle pad shape with Pin 1 Oblong Gang Mask



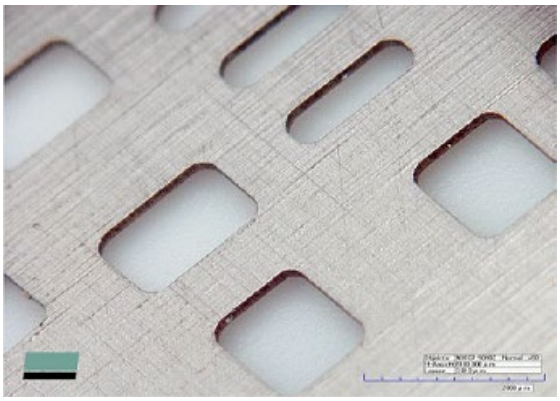
**e. RF Design Note**
For RF, microwave and high frequency controlled impedance traces, solder mask should be removed from above the transmission line. The solder mask alters the dielectric environment by replacing air (Dk ≈ 1) with mask resin (Dk ≈ 3–4), increasing effective Dk, adding loss, and disturbing the EM field distribution that defines the line's impedance. Mask thickness and moisture absorption further introduce variability. To maintain stable impedance and minimize RF loss, specify a solder mask keep-out over all RF microstrips, antennas, and matching network traces.

## 19.2 – Corner Rounding

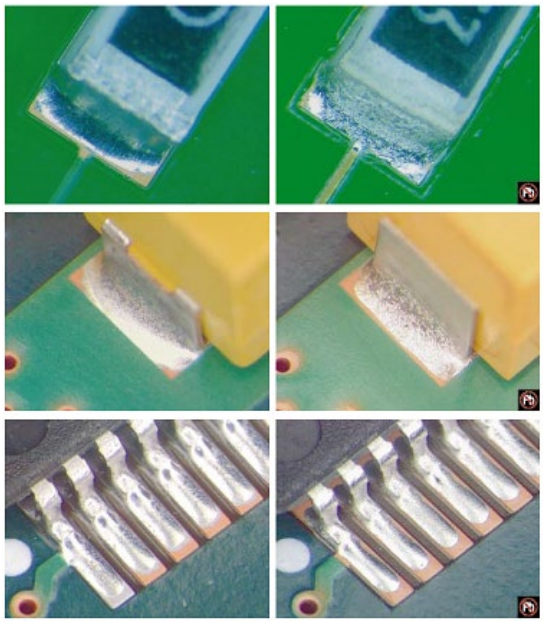
**a. Corner Radius Size (% of Pad Width) – 25%**
The 25% value is applied to every corner, that is equivalent to 50% of the pad width.

**b. Corner Radius Size Limit – 0.10**
The 0.10 default value sets the limit on the corner radius. Some component manufacturers recommended solder patterns indicate a 0.05 mm corner radius. The corner radius size limit is totally up to the PCB designer or CAD librarian. There is no recommended Standard for this radius limit. Some companies use a 0.15 – 0.20 Corner Radius Limit. Any value above 0.20 is excessive.

*Corner Radius Note:*
Some people say that rounded rectangle pad shape is best for lead free solder. This is a myth, as all pad shapes are OK with lead free solder. IPC has recommended Oblong pad shape since the release of IPC-SM-782 in March 1987. The 782 Standard had both text and graphic illustrations. The text referred to Oblong (or Full Radius) pad shape but the images portrayed Rectangle Pad Shape. This was confusing to the reader of the Standard. Most component manufacturers recommended patterns for surface mount parts illustrate Rectangular pad shape. The Rounded Rectangle Pad Shape is a compromise between the world standard Oblong and the component manufacturer Rectangle. Also, it is important to note that paste mask stencil aperture openings are laser cut with rounded corners. It makes sense to have the pad shape match the paste mask stencil aperture shape.

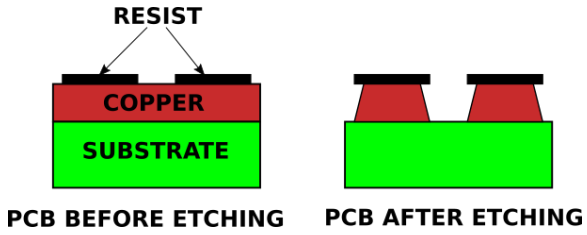


When the PCB goes through a reflow oven, the paste mask tends to gravitate toward the terminal lead and away from the pad corners. It doesn't make sense to have rectangular pad shapes with no solder in the pad corners. Here is a photo of both lead and lead-free solder with no solder in the corners.



## 19.3 – Manufacturing Tolerances

**Manufacturing Tolerances Note:**
Manufacturing tolerances have existed in the IPC mathematical model for surface mount pad size calculation since 1987. The **Fabrication Tolerance** was used to compensate for the etching process. But in the 1990's, the fabrication shops started to swell the outer layers to compensate for their etch back tolerances so that they could deliver pad sizes and trace widths the same size as the original Gerber data. But there is also an issue with the subtractive process where the etch acid gets slightly under the photo resist and creates a trapezoidal effect in the trace and pad. IPC-7351 uses a 0.05 mm fabrication value in the pad size math to compensate for this subtractive process. The average copper thickness on the outer layers is ½ oz. or 0.017 mm. The acid under photo resist undercut value is only a small percentage of that. Basically, the Fabrication Tolerance added to the pad size calculation is no longer applicable.




The **Assembly Tolerance** used in the IPC-7351 mathematical model for pad size calculation is 0.025 and established in 1987. This value was to compensate for the assembly machine placement accuracy. Today's advanced assembly machines place components with a 0.01 accuracy or less. The Assembly tolerance added to the pad size calculation is no longer applicable today.

When IPC developed the solder joint goals for IPC-7351, side goals for fine pitch semiconductor packages had to be set at negative values to compensate for the robust manufacturing tolerances. IPC-7352 turned off the manufacturing tolerances and updated every negative value in the Terminal solder joints to 0.00. By turning off the manufacturing tolerances and changing all negative solder joint goals to 0.00, the pad length & width size is only affected by +/-0.05.

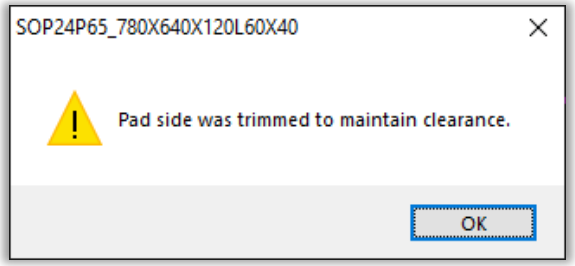
| Lead Part | Maximum (Most) Density Level A | Median (Nominal) Density Level B | Minimum (Least) Density Level C |
|---|---|---|---|
| Toe (J ) | 0.55 | 0.45 | 0.35 |
| Heel (J ) | **-0.05** | **-0.07** | **-0.10** |
| Side (J ) | **-0.05** | **-0.07** | **-0.10** |
| Round-off factor | Round off to the nearest two place decimal, i.e., 1.00, 1.05, 1.10, 1.15 | | |
| Courtyard excess | 0.50 | 0.25 | 0.10 |
| Resistor Chip Array Concave **RESCAV, CAPCAV, INDCAV, OSCSC** | | | |

**IPC-7352** changed the Fab & Assy Tolerances:

- **Fabrication Tolerance (+/-) = 0.00**
- **Placement Tolerance (+/-) = 0.00**

## 19.4 – Minimum Trim and Spacing

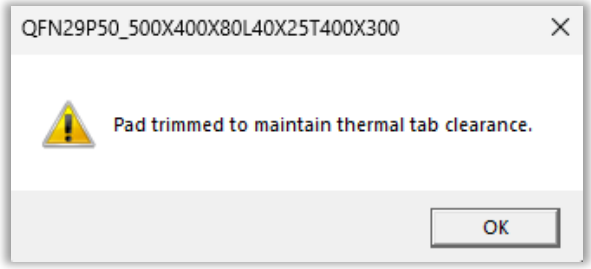
**a. Minimum Pad to Pad – 0.15**
The minimum pad to pad rule is intended for surface mounted parts. When the pad spacing violates this rule, Footprint Expert will automatically trim the pad to enforce this rule and an error message will be created that looks like this:



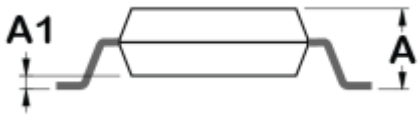

The value of 0.15 is arbitrary and not a hard-coded standard. The minimum pad to pad spacing rule should never violate your minimum PCB clearance rule. If your PCB layout is using a minimum trace/space rule of 0.20 mm then you should set the minimum pad to pad rule to 0.20.

Also, if you wanted to insure a 0.08 minimum solder mask web and your solder mask swell is 0.05 then change the value to 0.18. If the minimum pad to pad is 0.15 and the pads violate that rule, the Gang Mask feature will kick in and mask the entire row.

**b. Minimum Pad to Thermal Tab – 0.20**
The minimum pad to thermal rule is primarily established by the majority of component manufacturer's recommended patterns and not any industry Standard. If the thermal pad is too big and violates this rule, the pads will be trimmed, and a warning message will be created that looks like this:




**c. Minimum Trim Standoff Height – 0.03**
The minimum stand-off is the A1 package body bottom to PCB space dimension in gull wing packages.




The default "minimum" value of 0.03 mm will only trim pad Heel under the component package if the A1 value is less than 0.03. The main purpose for pad trimming under low profile packages is to eliminate paste mask from touching the plastic body during reflow. The pad Heel is an important part of the gull wing solder joint, but if the Heel pad is under a low profile package, the solder on the pad Heel is pushed out by the weight of the package creating excess solder.

IPC-J-STD-001 mentions in table 7-7 Dimensional Criteria – Flat Gullwing Leads. Note 4: Solder should not extend under the body of surface mount components whose leads are made of Alloy 42 or similar metals.

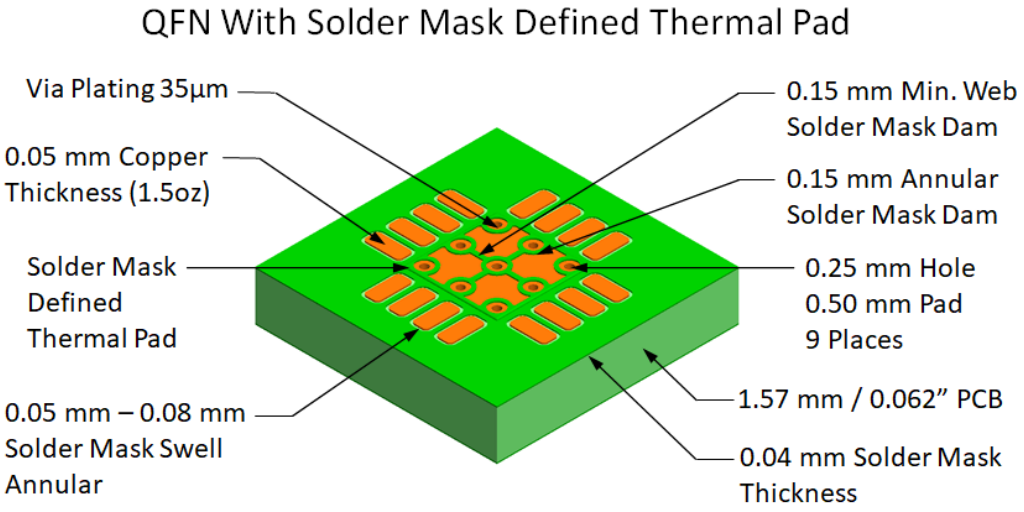
## 19.5 – Thermal Tabs

**a. Solder Mask Expansion +/- 0.00**
Typically, the thermal tab solder mask is 1:1 scale of the pad size. It's OK for the fabrication solder mask tolerance to be +/- 0.05 that could result in the solder mask creeping over the thermal pad. The minimum paste mask aperture is 0.10 mm from the edge of the thermal pad. Most component manufacturers recommend a 1:1 scale solder mask on thermal pads.

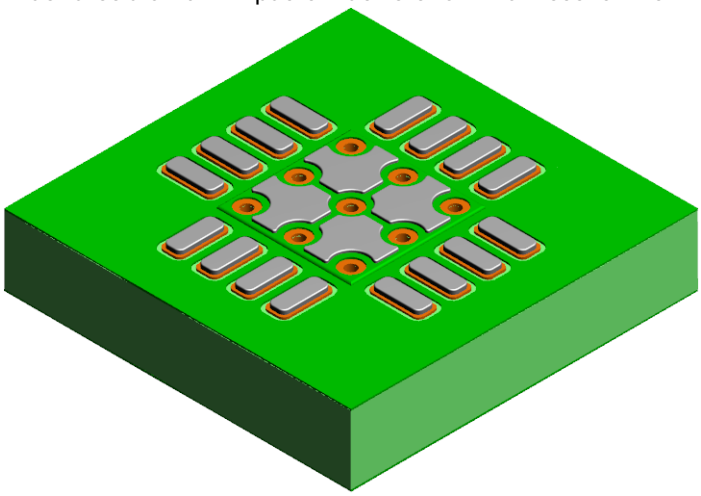
**b. Pattern Defined Solder Mask – on/off check box**
The default setting for this feature is turned off because the user must accept the responsibility for turning it on. The solder mask defined thermal pad places solder mask in-between the paste mask apertures, basically damming in the paste mask from flowing. The IPC-7093A describes all the benefits of this feature.

Ability to add vias in the solder mask area and the paste mask will not flow down the via hole. This could potentially save on fabrication costs to avoid via plugging to stop the flow of paste mask into the via hole.

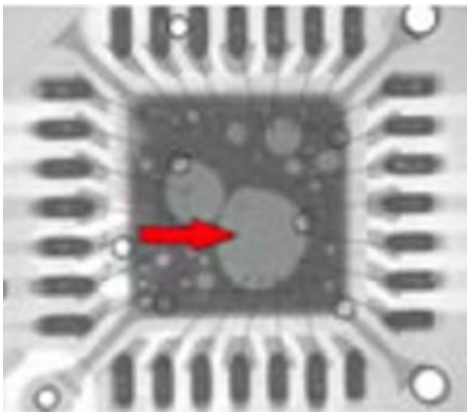
This image provides some basic values for defining a solder mask defined thermal pad.




This image illustrates a 0.10 mm paste mask stencil thickness for the image above.



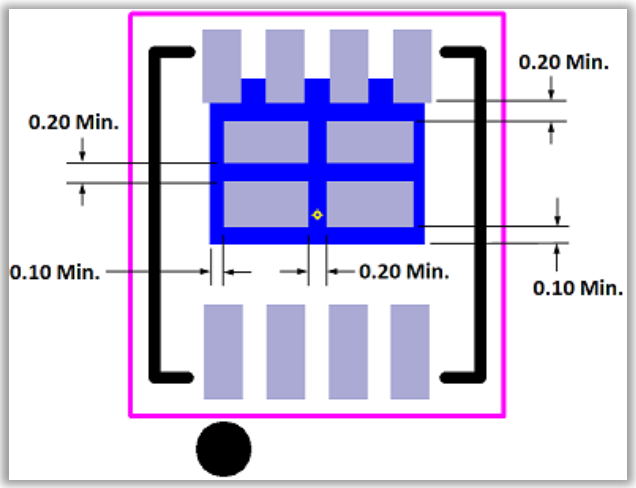
Because the paste mask is dammed in by solder mask, this reduces paste mask voiding because the solder has nowhere to flow. The amount of voiding post reflow should not exceed 25% per IPC-A-610. Voiding occurs when the thermal pad is not solder mask defined.



**c. Paste Mask % – 60%**
The default setting is 60% paste mask coverage. IPC-7093A figure 3-10 recommends that the stencil design provide 60 – 70% solder paste coverage on the thermal pad area.

**d. Minimum Intra-Pattern Pattern Space – 0.20**
The default setting for this feature is 0.20 mm. It is important to have a minimum stencil aperture spacing to increase the stencil web strength. This will make the stencil last longer and work better.

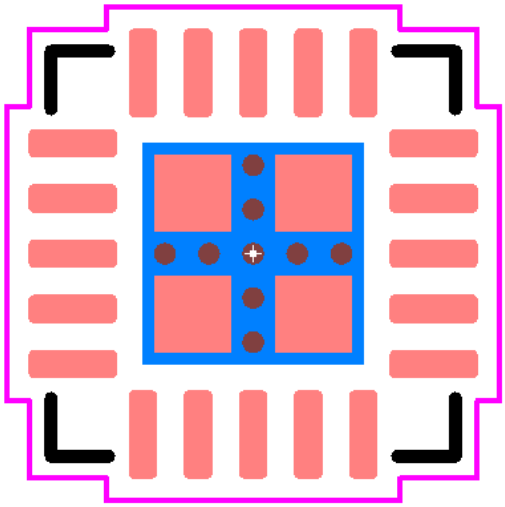
**e. Minimum Pattern to Pad Edge Space – 0.10**
The default setting for this feature is 0.10 mm. This setting works OK up to 70% paste mask coverage. If you need 80% paste mask coverage, you will need to set this value to 0.00 to allow paste mask to extend to the edge of the pad. If you keep the 0.10 paste to pad edge and have 80% paste mask coverage, the checkerboard pattern will turn into a single aperture.




If you use the solder mask defined thermal pad feature and intend to place vias in-between the paste mask you need to figure out the via hole size and add 0.10 for the minimum pattern space. Example: if the via hole size is 0.20 + 0.10 clearance for the solder mask web, then the thermal tab minimum pattern space should be set to 0.30. Or you can move the calculator part to FP Designer and edit the pad stack paste mask to set the aperture size and spacing.

*Note 1:* The Solder Mask and Paste Mask aperture opening are the same size and location.

*Note 2:* 9 vias provide the maximum thermal relief for most packages with thermal tabs.



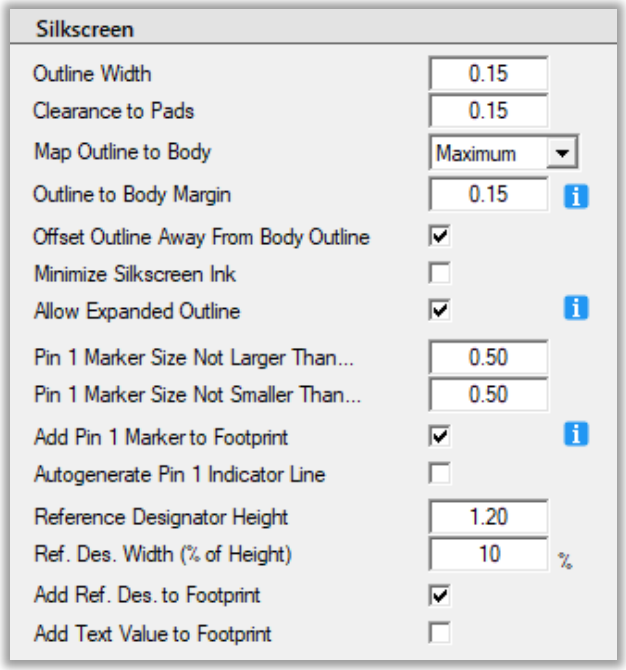
## 19.6 – SMD and TH Miscellaneous

**Cathode/Anode Pin Names – Alphanumeric or Numeric**
The default setting is Alphanumeric and produces pin names A & C. This setting is primarily used for schematic symbols that support Alphanumeric pins. The preferred pin label assignments for Diodes and LED's are C and A for Cathode and Anode. This avoids making a mistake between the schematic symbol and the CAD library. But if you use numeric pin names on these polarized devices, you must make sure that the schematic symbol pins 1 & 2 match the PCB footprint pins 1 & 2. You can also rename Diode and LED pins to any alphanumeric value to match the schematic.

# 20.0 – Drafting Outlines & Polarity Marking

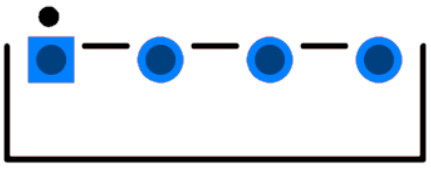
**Overview**
PCB drafting outlines and polarity markings are critical for preventing component failure, rework, and assembly errors. Proper drafting requires clear component boundaries (silkscreen outlines), exact Pin-1 markers for ICs, and unambiguous anode/cathode (or positive/negative) indications for polarized devices.

## Silkscreen Drafting Options

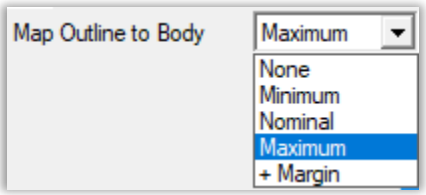



**General:** Silkscreen is a non-conductive ink layer applied to provide visual guidance for assembly, testing, and maintenance.

**Outline Width:** default settings can be changed to your company standard. Fabrication minimum silkscreen line width is 0.10. The nominal line width is 0.15 and maximum line width is 0.20 (but any value above 0.10 is acceptable). Clearance to Pads: Defines the minimum allowable space between calculated silkscreen outlines and adjacent pads or applied to clearance between silkscreen articles. To avoid this violation lines may be terminated or trimmed. Polarity indicator placement may be adjusted.



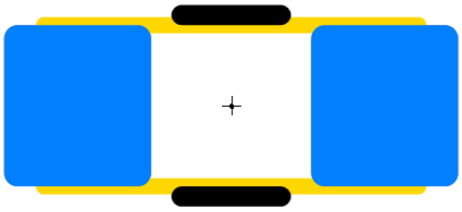
**Map Outline to Body:** This drop-down menu sets the size of the silkscreen outline relative to the component body. The "Margin" option is applied in conjunction with the Outline to Body option. The default value is "Maximum".



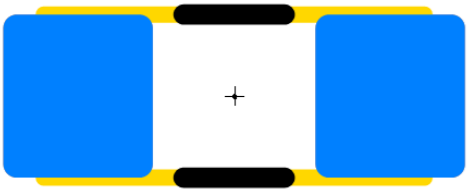

**Outline To Body Margin:** Defines the silkscreen outline-to-nominal body spacing when "+Margin" is selected.

**Offset Outline away from Body Outline:** When checked, the silkscreen size is offset by an additional ½ line width to minimize the chance of obscuration by a component body.

**When Checked:**

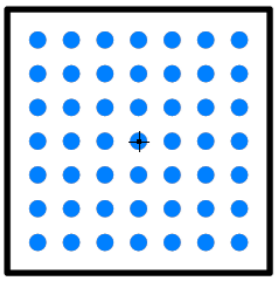


**When Unchecked:**

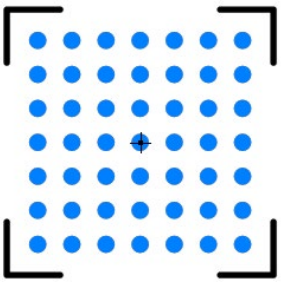


**Minimize Silkscreen Ink:** When this option is checked, the Grid Array silkscreen outlines will be hatched. When it is unchecked, the silkscreen outline will be a full body outline.

**Minimize Silkscreen Off**

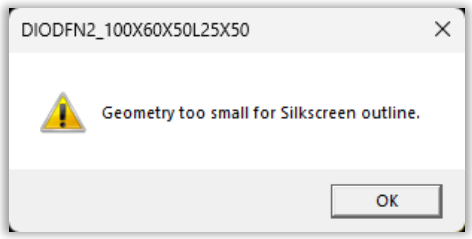


**Minimize Silkscreen On**

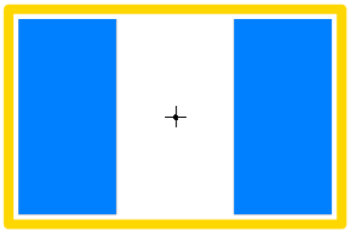


**Allow Expanded Outline:** Allows expansion as required in order to add an outline to micro-miniature parts.

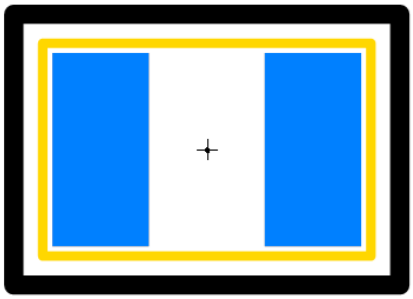
**Error message when Expanded Outline Off:**




**Expanded Outline Off:**



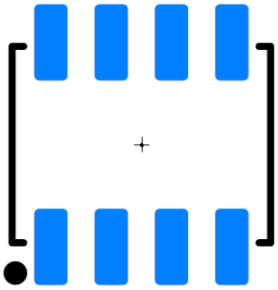
**Expanded Outline On:**



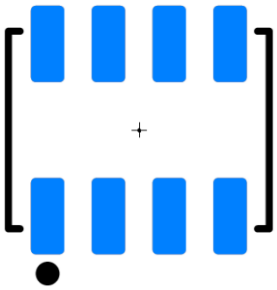
**Pin 1 Markers General:** Markers are only added to parts having a polarity. For example, Diodes and polarized capacitors may have polarity, resistors and inductors do not have polarity and can be inverted during assembly.

**Pin 1 Marker Size Not Larger/Not Smaller Than:** The silkscreen polarity dot size is automatically calculated to adjust to the component while maintaining a size within the range of these two values. Making the values equal results in a fixed dot size.

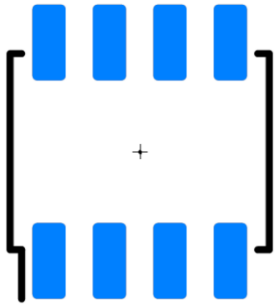
**Add Pin 1 Marker to Footprint:** Enables or disables the automatic addition of polarity dot markers. Silkscreen polarity markers are placed to conform to the drafting settings and component physical constraints. If the automatic placement is found to be unacceptable, you can manually add Polarity Symbols.



When the pads are too short or under the package, a pin 1 dot at the end of the pad is acceptable.



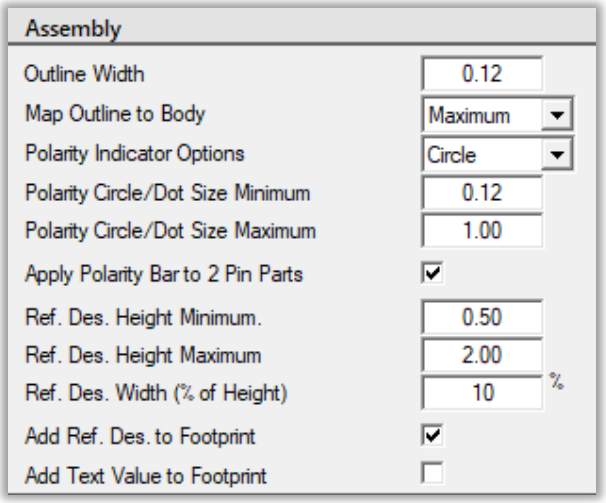
Autogenerate Pin 1 Indicator Line: Enables the addition of a line next to pin1 on some parts, typically ICs.



**Reference Designator Height and Width:** Fonts are not an option owing to differences in CAD translator options, so FPE uses height as a dimension with a percentage of height defining pen width. The effect of width can't be observed in FPE.

**Add Reference Designator to Footprint:** Enables or disables the Reference Designator for a translated output. Add Value to Footprint: Enables or disables an additional silkscreen text "Value" for a translated output.

## Assembly Drafting Options



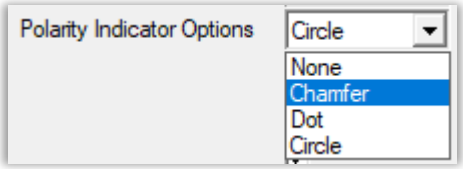

**General:** Assembly layer drafting elements provide visual and dimensional details that guide component placement, orientation, and verification. Assembly layers and are critical for manufacturing accuracy.

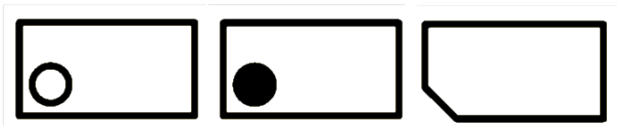
**Outline Width:** The assembly outline never gets manufactured, so the line width is user definable.

**Map Outline to Body:** This drop-down menu sets the size of the silkscreen outline relative to the component body.

The default value is “Maximum”.

## Polarity Indicator Options:



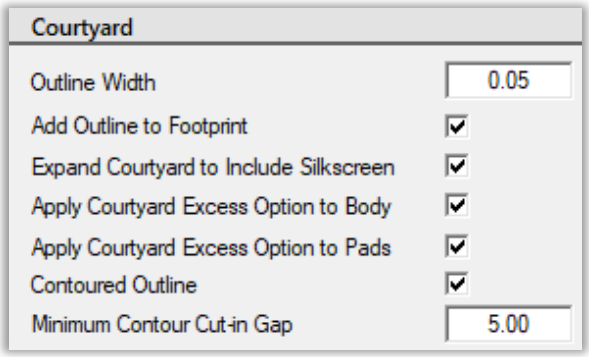
**Pin 1 Dot/Circle Size Not Larger/Not Smaller Than:** The silkscreen polarity dot size is automatically calculated to adjust to the component while maintaining a size within the range of these two values. Making the values equal results in a fixed dot size. The Chamfer also automatically adjusts the component size to maintain a size within the range of 1/3 the lesser of body height or width, not to exceed 1 millimeter.

**Add Polarity Bar To 2 Pin Parts:** When checked, polarity Indicator options are replaced by wide line at the pin 1 location of polarized 2 pin parts.

**Reference Designator Height Minimum and Maximum:** Text values are automatically calculated to fit within the assembly outline while maintaining a size within the range of these two values. Making the values equal results in a fixed dot size. Fonts are not an option owing to differences in CAD translator options, so FPE uses height as a dimension with a percentage of height defining pen width. The effect of width can’t be observed in FPE.

**Add Reference Designator to Footprint:** Enables or disables the Reference Designator for a translated output. Add Value to Footprint: Enables or disables an additional assembly text “Value” for a translated output.

## Courtyard Options

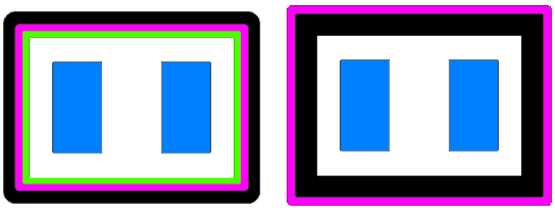



**General:** A courtyard defines the minimum clearance area around a component’s footprint to ensure manufacturability, assembly, and rework-ability. It is not part of any electrical circuit but is critical for mechanical and process requirements. The courtyard to body is mapped to the maximum package dimensions.

**Outline Width:** User definable.

**Add Outline to Footprint:** Enables or disables addition of the Courtyard to the footprint.

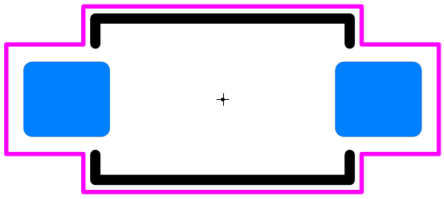
**Expand Courtyard to Include Silkscreen:** Allows expansion of the Courtyard to encompass the Silkscreen outline in situations where the Silkscreen size exceeds the Courtyard.



**Apply Courtyard Excess to Body/Pads:** When checked, does not add the excess over body, or pads respectively, to courtyard. Note: The *Expand Courtyard to Include Silkscreen* is not affected by this option.

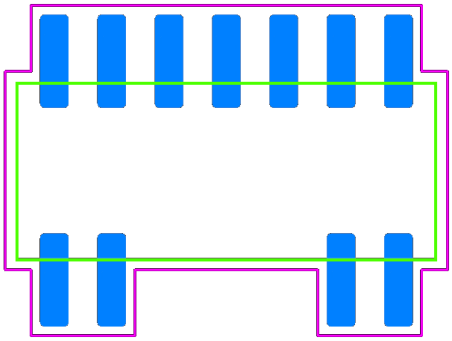
**Courtyard Excess values:** These values are not found in the Courtyard Drafting Options but are included with Terminal Options and, as such, unique to each terminal type – grid arrays, surface mount and thru-hole.

**Contoured Courtyard:** When checked, allows the Courtyard to conform to irregular shapes that might be present in the footprint.

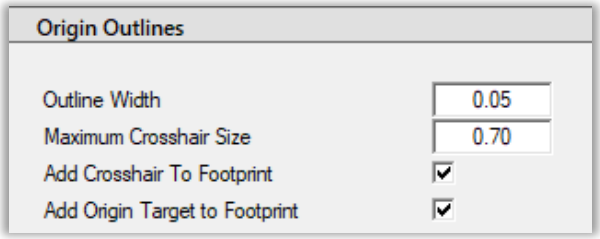


**Rectangular Courtyard:** This was the original IPC-SM-782 courtyard shape.

**Minimum Cut in Gap:** This option defines the minimum size of a space that can included by a Courtyard contour. Values smaller than this size will be ignored by the contour.



## Origin Options




**General:** An Origin construct defines a visual, physical reference indicating a point from which all other footprint dimensions may be referenced. The Origin construct consists of two independent drafting features forming a crosshair and circle.

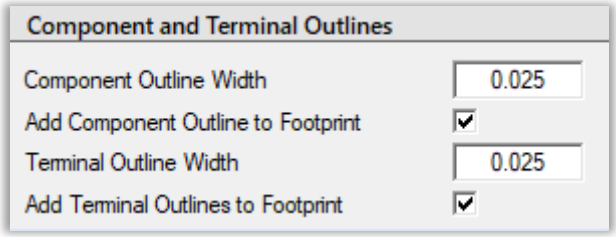
**Outline Width:** user definable as there is no industry standard.

**Maximum Crosshair Size:** defines the maximum length of a crosshair line (plus the outline width). As a footprint shrinks, the crosshair size is reduced in proportion to the courtyard.

**Add Crosshair to Footprint:** When checked allows an origin crosshair to be added to a footprint.

**Add Target to Footprint:** When checked allows an origin target to be added to a footprint.

## Component and Terminal Options




**General:** Component and terminal outlines are always shown in the nominal material condition. This is done to maintain a consistent relationship that prevents confusing overlapping outlines that would occur with mixed material conditions.

**Component Outline Width:** User definable.

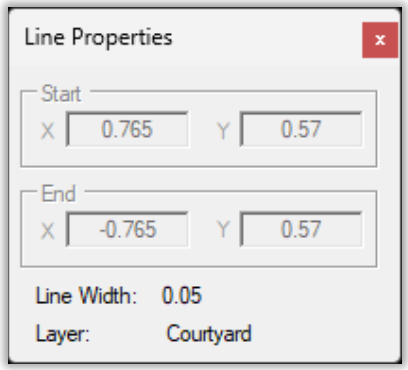
**Add To Footprint:** When checked, allows the nominal component body outline to be added to a footprint.

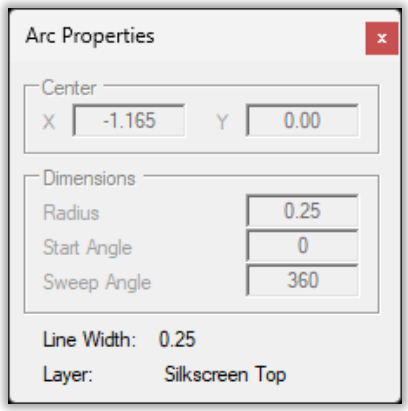
**Terminal Outline Width:** User definable. This feature is used for visibility of the terminal lead on the pad. If the terminal lead is not 100% on the pad, there is something wrong with the dimensions.

**Add To Footprint:** When checked, the nominal terminal outlines to be added to the footprint.

## Drafting Element Properties

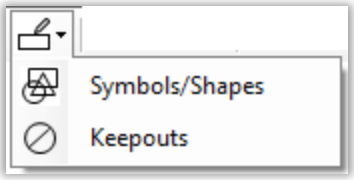
**General:** Right-clicking on any of the drafting items will open a dialog box, appropriate to the selected item, displaying its characteristics for viewing only.




## Symbol and Keep-out Creation Tools

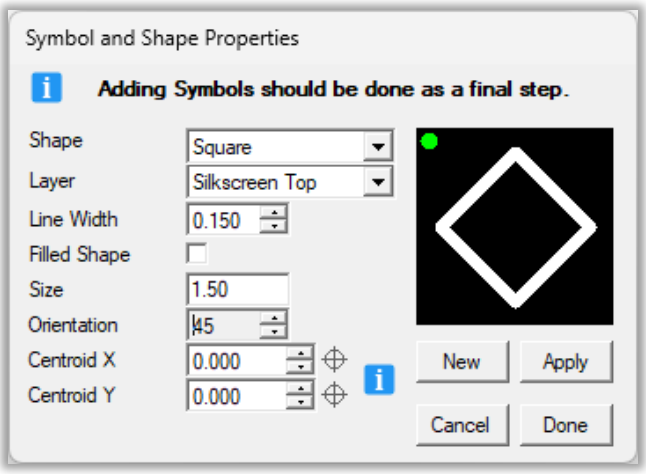
The Symbol and Keep-out Creation Tools provide the means for manual design and placement of drafting elements that do not lend themselves to an automatic Calculator function. The tools are activated from a drop-down button on the Footprint Viewer toolbar.



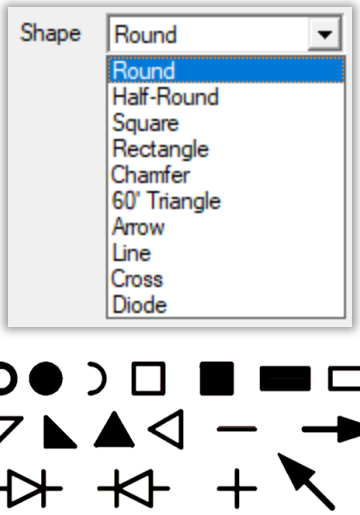

**Symbol/Shapes and Keep-outs:** Clicking either drop-down item Opens the Symbol Shape or Keep-out Properties Dialog Boxes respectively.

**Note:** Adding drafting symbols should be done as a final step in footprint creation. Symbols and keep-outs are typically placed in releation to other footprint features. Therefore any time a component specification, rule or drafting element is changed, all manually added symbols and Keep-outs are deleted. However, once added, sysmbols and keep-outs are saved to the FPX library with the footprint.

## Drafting Symbol Creation

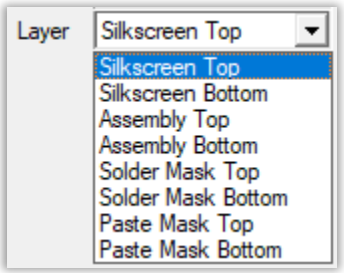



**Shape:** The following illustrates a variety of available symbol shapes. Shapes can be configured for line width, size, fill, orientation and placement.






**Layer:** Selects the layer assignment for symbols. Some symbols, such as Diode and Arrow can only be added to silkscreen and assembly layers.



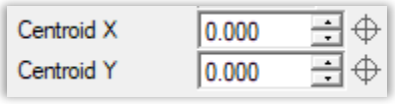
**Outline Width:** Silkscreen and assembly symbol line width should match the master line widths.

**Fill:** When checked, creates a solid feature. Fill is not available for diodes or half circles.

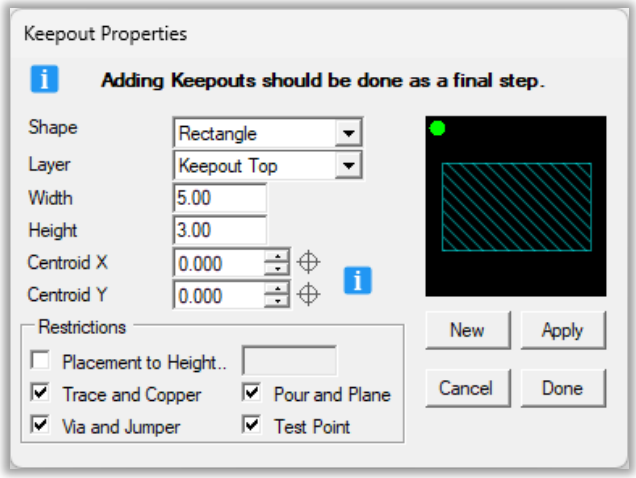
**Size:** This option can be specified in one of three ways: Diameter, for round features; Height and Width, for square and rectangular features; Size for Line, Cross, Chamfer, 60' Triangle and Diode; Base (the arrow base) for Arrow.

**Orientation:** This option may be specified, with limitations, to some shape types.

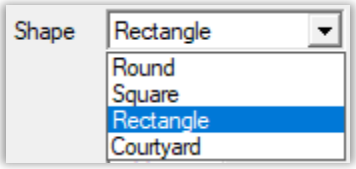
**Placement X and Y:** The X and Y numeric controls may be used to locate or relocate the symbol. Clicking on one of the "target" icons resets the value to zero. The F2 key may be used to capture an X-Y location prior opening the Symbol menu.



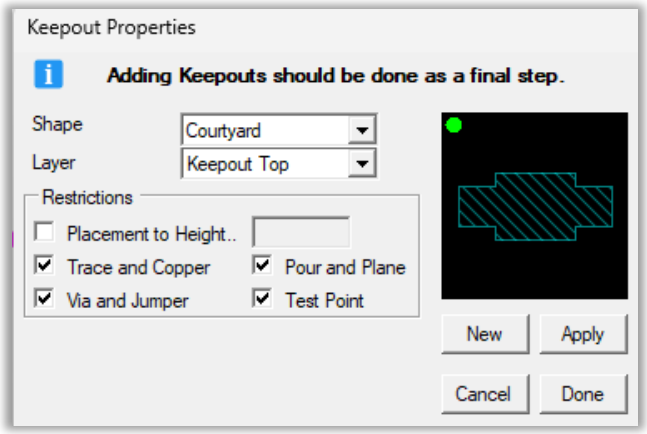

## Keep-out Creation

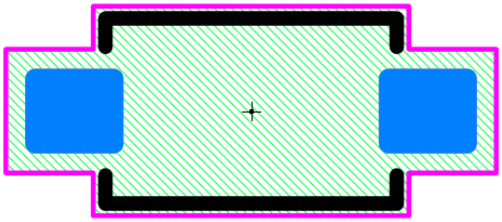



**Shape:** Basic Keep out available shapes are round, square and rectangular.

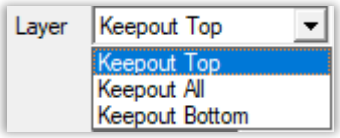



A notable exception is the Courtyard option. This option creates a keep out that mirrors the courtyard allowing restrictions that can be applied to the entire footprint.

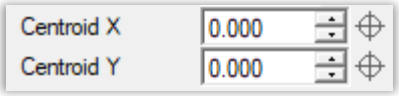


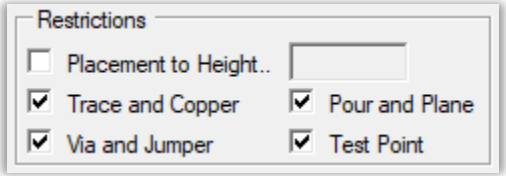
**Layer:** Selects the layer assignment for keep outs.




**Placement X and Y:** The X and Y numeric controls may be used to locate or relocate the keep-out. Clicking on one of the "target" icons resets the value to zero. The F2 key may be used to capture an X-Y location prior opening the Keep-out menu.




**Restrictions:** Defines the feature types that will not be allowed within the keep-out area. *Placement Height* is the maximum allowable height of any object within keep-out area.



## Symbol and Keep-out Properties

**Apply:** This button will add a highlighted current symbol or keep-out feature to the footprint. When highlighted, the feature will continue to be subject to changes made and can be updated any time buy click apply.

**New:** This button will instantiate an applied feature and initiate a feature of the same type (symbol or keep-out). This makes it unnecessary to close and reopen a menu in order to define and add a new feature.

**Cancel:** This button will abort any feature currently in progress and return to the start menu configuration.

**Done:** Closes the feature's menu. Upon closing, a reminder message will be displayed for features that have not been applied.

**General:** Right-clicking on any symbol or keep-out feature will allow selection of a *Properties* dialog box, which just happens to be the Creation tool menu, allowing a full editing capability of the selected feature.

# 21.0 – Package and Terminal Tolerances

Component and Terminal tolerances affect the resulting pad stack size and spacing. Many component manufacturer package and terminal tolerances are too robust and unrealistic. Especially in component datasheets that are 20 – 30 years old. The machines that produce today's component packages are fairly accurate and it's the manufacturers' goal to produce component packages in the Nominal Material Condition. The IPC-7352 mathematical model is 100% dependent on package tolerances to form the solder joint goals for assembly attachment to accommodate the package in all 3 material conditions for Least, Nominal and Most.

PCB component package tolerances account for variations in manufactured electronic component dimensions, ensuring that physical parts safely fit on their designated circuit board footprints. Every electronic component has minor sizing variations due to material changes, tooling wear, and thermal expansion during assembly. Circuit designers must accommodate these variations when building CAD libraries to prevent assembly failures, bad solder joints, or physical placement collisions. When a semiconductor component manufacturer datasheet with package dimensions only provides Nominal dimensions for the Body Length and Width the PCB librarian must assign a 0.10 mm minimum, 0.15 mm nominal or 0.20 mm maximum tolerance.

Terminal Tolerances vary. But the range averages between 0.10 and 0.20, same as package tolerances.

| Package | Terminal Tol. Range |
|---|---|
| SOIC 1.27 Pitch | 0.40 - 0.45 |
| SOP 0.80 Pitch | 0.15 - 0.20 |
| SOP 0.65 Pitch | 0.15 - 0.20 |
| SOP 0.50 Pitch | 0.10 - 0.15 |
| QFP 0.80 Pitch | 0.15 - 0.20 |
| QFP 0.65 Pitch | 0.15 - 0.20 |
| QFP 0.50 Pitch | 0.10 - 0.15 |
| QFN 0.80 Pitch | 0.15 - 0.20 |
| QFN 0.65 Pitch | 0.10 - 0.15 |
| QFN 0.50 Pitch | 0.10 - 0.15 |
| QFN 0.40 Pitch | 0.10 - 0.15 |
| Chip 01005 | 0.03 |
| Chip 0201 | 0.05 |
| Chip 0402 | 0.10 - 0.15 |
| Chip 0603 | 0.15 - 0.20 |
| Chip 0805 | 0.20 - 0.30 |
| Chip 1206 | 0.15 - 0.25 |

IPC-7351B refers to a mathematical model that also includes Fabrication and Assembly tolerances. IPC-7352 does not consider these tolerances.

The mathematical model takes into consideration the minimum and maximum package and terminal dimensions to ensure that the resulting land pattern accommodates the package tolerance range. Tolerances are referred to as Min/Max technology. This means the pad stack size and spacing will accommodate the component package in the minimum or maximum material condition.

Since the package and terminal tolerances affect the resulting pad stack size and spacing, robust tolerances will produce larger pad stacks while no tolerances will produce pad stacks that are too small. The IPC-7351 Side solder joint goal for chip packages is zero. The pad width is the same dimension as the Maximum terminal lead width.

When the Heel Solder Joint Goal for chip packages is zero, the heel goal is determined by the terminal lead and package length tolerances.

The Toe normally has a solder joint goal has a predefined value. Then the terminal lead and package length tolerances are added to the Toe value. The resulting Toe solder joint is a combination of the Toe goal value and terminal and package length tolerances.

The goal is to have one Case Code footprint for every resistor in your supply chain. If you have 10 resistor suppliers and they provide different tolerances, to achieve this goal, standard tolerances that can accommodate all 10 vendors packages must be documented.

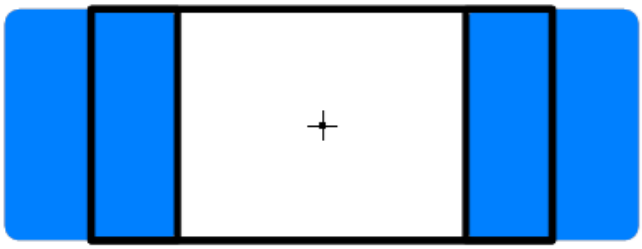
Because every component family has a unique 3D STEP model, it's necessary to create a footprint for each component family. Inductor, Resistor, Capacitor, Diode, etc. all have unique 3D STEP models.

Recommended Package tolerances for chip case codes:

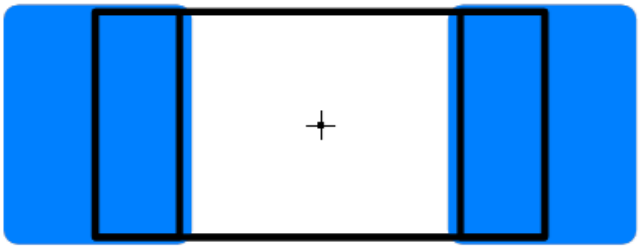
- 01005 – 0.02 mm
- 0201 – 0.03 mm
- 0402 – 0.05 mm
- 0603 – 0.10 mm
- 0805 – 0.15 mm
- 1206 and higher – 0.20 mm

Different component manufacturers will publish a wide range of tolerances. For example, Panasonic, Yageo, Vishay, AVX, Murata, Kemet and Taiyo Yuden will have different tolerances to the same Case Code. But the PCB designer or CAD librarian want one set of tolerances for each Case Code.

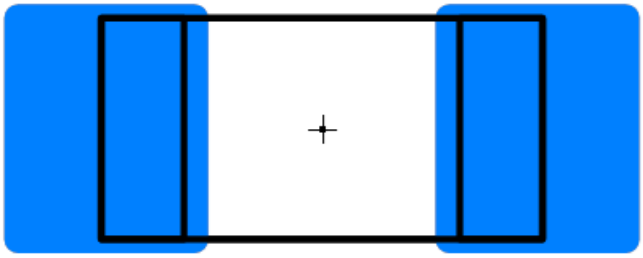
Here is a 0603 Chip with no tolerances:



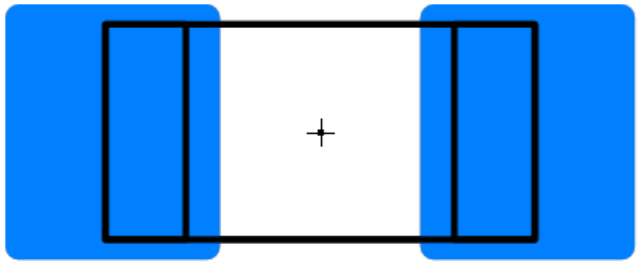
Here is a 0603 Chip with a 0.05 tolerance on Length, Width and Terminal Nominal Density Level:



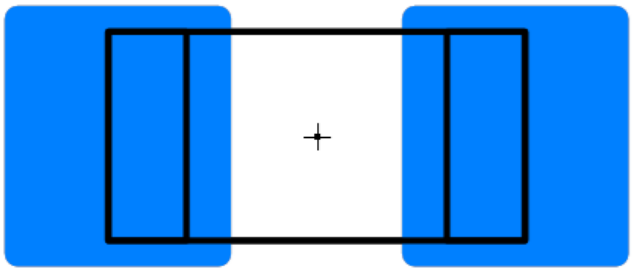
Here is a 0603 Chip with a 0.10 tolerance on Length, Width and Terminal Nominal Density Level. This is the optimal footprint pattern.



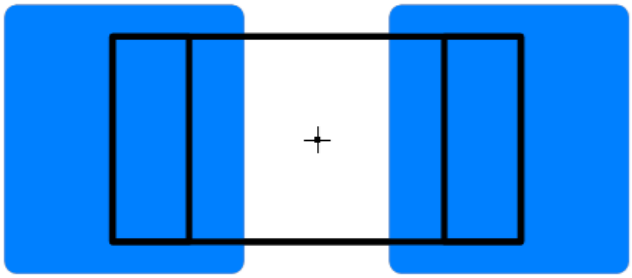
Here is a 0603 Chip with a 0.15 tolerance on Length, Width and Terminal Nominal Density Level, Slightly robust.



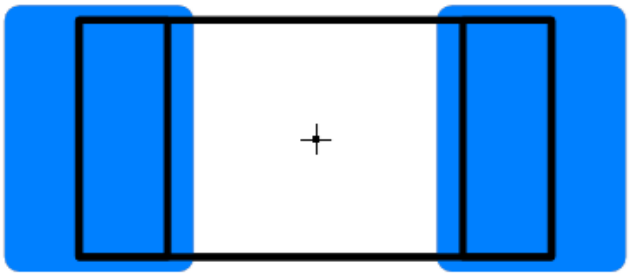
Here is a 0603 Chip with a 0.20 tolerance on Length, Width and Terminal Nominal Density Level. Too robust.



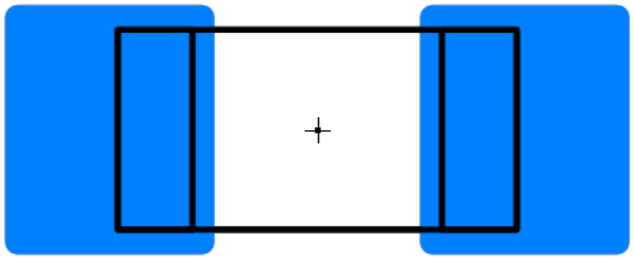
Here is a 0603 Chip with a 0.25 tolerance on Length, Width and Terminal Nominal Density Level. Grossly robust.



Here is a 0603 Chip with a 0.10 tolerance on Length, Width and Terminal for **IPC Least Density Level**:



Here is a 0603 Chip with a 0.10 tolerance on Length, Width and Terminal for **IPC Most Density Level**:



Chip component manufacturers do not use their package tolerances when publishing their manufacturer recommended patterns in their datasheets. They use nominal package dimensions and add a Toe, Heel and Side solder joint regardless of how robust their tolerances are. If component tolerances are real and component packages can be shipped to assembly shops and some come in the minimum material condition and some come in the maximum material condition, there will be assembly attachment issues. Beware of component manufacturers recommended solder patterns. Make sure they can accommodate the tolerances provided in their datasheet.

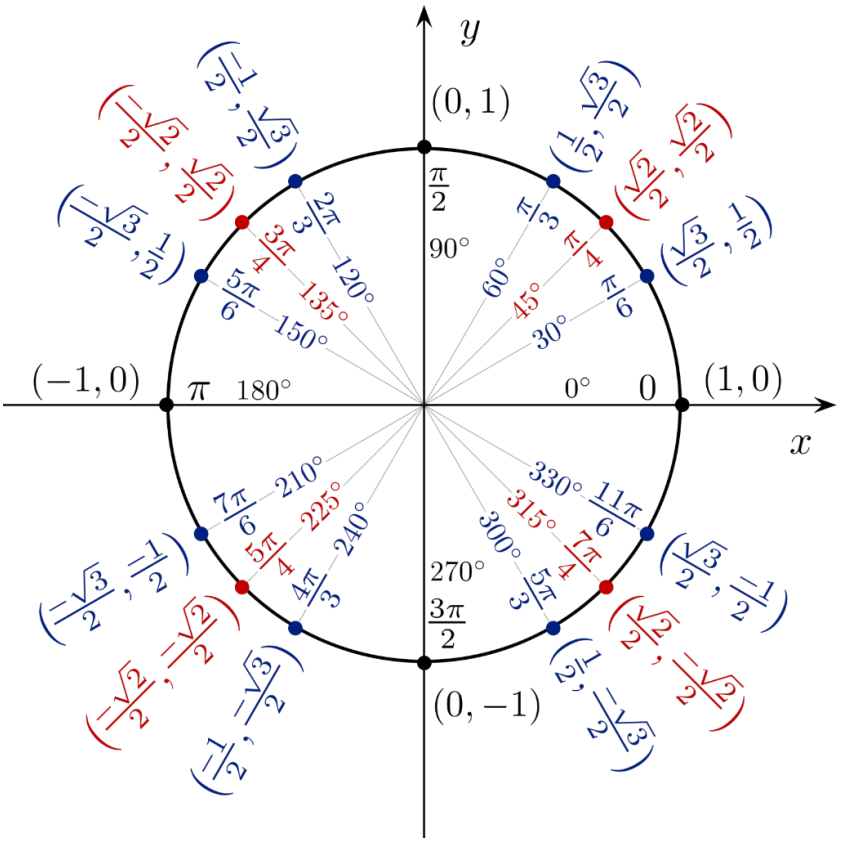
In the future, component package tolerances will be very small and even nonexistent. When this happens, the IPC-7352 Mathematical Min/Max model becomes obsolete. When component packages are produced without tolerance, a new model for calculating pad stacks must replace the IPC-7352 math. The Nominal calculation mode only requires nominal component package dimensions and solder joint goals for Toe, Heel and Side. Currently, many IPC-7352 Heel and Side solder joint goals are 0.00 and the Heel and Side goals rely 100% on package tolerances. When package tolerances are 0.00 the solder joint goals for Heel and Side must be updated to values that are consistent across all terminal lead forms.

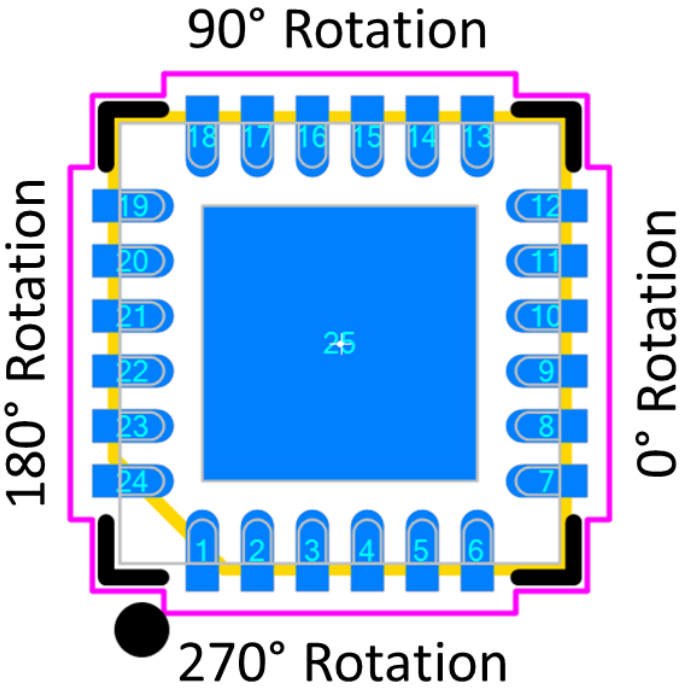
# 22.0 – Zero Component Orientation

Printed circuit board technology uses geometry to define the rotational angle of every object in the PCB design. Objects use geometry to define the orientation starting at 0,0 which is located on the right center. Cartesian coordinates are also defined per the PCB or Footprint origin. Popular Pad and Footprint rotations are 0, 90, 180 and 270 degrees, but can be placed at any angle. Pad and Footprint orientations start at 0,0 and rotate counterclockwise.

Pad Rotations Start at 0,0 in the Positive X Location

Pad rotation follows geometry standards.




Footprint rotations are in 90° increments starting with the zero-component orientation per the IEC 61188-7 Rotation B released in 2007 with pin 1 in the Lower Left corner. IEC 61188-7 reflects the same zero component orientation documented in the IPC-SM-782 standard that was released in March 1987.

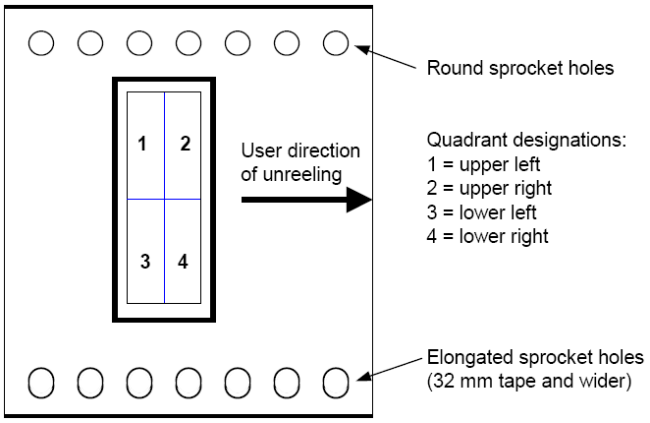
The main reason to establish and follow a zero-component orientation is to help automate the assembly process. A known zero-component orientation will eliminate hours of research in PCB assembly trying to figure out the footprint rotations in the CAD library.

In 2005, IPC-7351 introduced a new Zero Component Orientation with Pin 1 in the Upper Left, redefining pin 1 orientation to the Upper Left, and deviating from an 18-year old standard (1987 – 2005), defining the pin 1 orientation in the lower left. Also, the zero-component orientation should follow the Tape and Reel, Tube and Tray orientations defined by EIA. However, component manufacturer rotations vary from one mfr. to another for the same package type. A standard must be adhered to by component manufacturers.

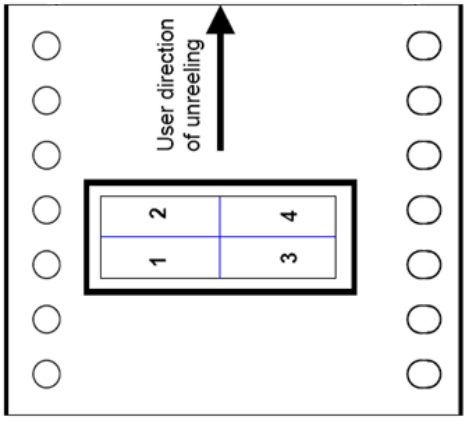
Here are the zero component orientations from IPC-7351, IEC 61188-7 and EIA-481-D.

| Component Family | IPC-7x51 | IEC 61188-7 | EIA-481-D |
|---|---|---|---|
| Chip (All Families) | Polarization On Left | Polarization On Left | Polarization On Left |
| Tantalum Capacitor | Polarization On Left | Polarization On Left | Polarization On Left |
| Molded Body Diode | Polarization On Left | Polarization On Left | Polarization On Left |
| SODFL | Polarization On Left | Polarization On Left | Polarization On Left |
| MELF | Polarization On Left | Polarization On Left | Polarization On Left |
| Aluminum Capacitor | Polarization On Left | Polarization On Left | Polarization On Left |
| Precision Inductors | Left | Left | Left |
| PLCC Square | Upper Center | Left Center | Left Center |
| PLCC Rectangle | Upper Center | Left Center | Left Center |
| LCC | Upper Center | Left Center | Left Center |
| QFP Square | Upper Left | Lower Left | Upper Left |
| QFP Rectangle | Upper Left | Lower Left | Lower Left |
| Bump QFP Side | Upper Left | Lower Left | Upper Left |
| Bump QFP Center | Upper Center | Left Center | Left Center |
| Ceramic QFP | Upper Left | Lower Left | Upper Left |
| SOIC | Upper Left | Lower Left | Lower Left |
| TSOP | Upper Left | Lower Left | Lower Left |
| TSSOP & SSOP | Upper Left | Lower Left | Upper Left |
| TSO8 (Mini US8) | Upper Left | Lower Left | Lower Right |
| BGA Square | Upper Left | Lower Left | Lower Left |
| BGA Rectangle | Upper Left | Lower Left | Lower Left |
| SOJ | Upper Left | Lower Left | Lower Left |
| CFP | Upper Left | Lower Left | Lower Left |
| QFN Square | Upper Left | Lower Left | Upper Left |
| QFN Rectangle | Upper Left | Lower Left | Lower Left |
| Chip Array | Upper Left | Lower Left | Lower Left |
| DFN | Upper Left | Lower Left | Lower Right |
| SON | Upper Left | Lower Left | Lower Right |
| SOT23-3 | Upper Left | Lower Left | Lower Right |
| SOT23-5 | Upper Left | Lower Left | Lower Right |
| SOT23-6 | Upper Left | Lower Left | Lower Right |
| SOT89 | Upper Left | Lower Left | Lower Right |
| SOT223 | Upper Left | Lower Left | Lower Right |
| SOT143 | Upper Left | Lower Left | Lower Right |
| SOTFL | Upper Left | Lower Left | Lower Right |
| SOT143 Reverse | Lower Left | Lower Left | Lower Left |
| TO-252 | Upper Left | Lower Left | Upper Left |
| TO-263 | Upper Left | Lower Left | Upper Left |
| LGA Square | Upper Left | Lower Left | Lower Left |
| LGA Rectangle | Upper Left | Lower Left | Lower Left |
| CGA Square | Upper Left | Lower Left | Lower Left |
| Oscillator (Multi-pin) | Upper Left | Lower Left | Lower Left |
| Crystal (2-pin) | Left | Left | Left |
| SMT Connectors | Left | Left | Left |
| PTH Connectors | Left | Left | Left |
| DIP | Upper Left | Lower Left | Lower Left |
| SIP | Left | Left | Left |
| Axial Lead | Polarization On Left | Polarization On Left | Polarization On Left |
| Radial Lead | Polarization On Left | Polarization On Left | Polarization On Left |
| PGA | Upper Left | Lower Left | Lower Left |

**EIA-481-D Tape and Reel Quadrant Designations**




**EIA-481-D**




**CAD Library Zero Orientation Quadrants**

Per all the JEDEC standard package definitions, quadrant 1 is where pin 1 should be located.

IPC and IEC use consistent rotations throughout their standard where EIA uses multiple rotation variations:
IPC-7x51 uses Quadrant 2 for Pin 1 Upper Left and Quadrants 2-4 for Upper Center
IEC 61188-7 uses Quadrant 1 for Pin 1 Lower Left and Quadrants 1-2 for Left Center
EIA-481-D uses Quadrant 1 for Pin 1 Lower Left BGA, SOIC, SOP, SSOP, QFNR, DIP
EIA-481-D uses Quadrant 2 for Pin 1 Upper Left TO-252, TO-263, QFNS, TSSOP
EIA-481-D uses Quadrant 3 for Pin 1 Lower Right for all SOT and miniature parts
EIA-481-D uses Quadrants 1-2 (Pin 1 Left Center) for PLCC, LCC

None of the 3 standards use Quadrant 4 for Pin 1 location.

This study concludes that the Zero Component output Orientation in the IPC Calculator should be 100% definable to allow the user to output any of the three industry standard rotations for CAD library construction. The only alternative is for the three standards organizations to collaborate on a single standard for the future.

The IPC Calculator is being used all over the world. In the USA, military contractors, including General Dynamics in Canada, are asking for the IPC Calculator to output CAD library parts in the EIA-481-D rotation. In Japan, Germany, Australia and South Korea, IPC Calculator users are asking to output CAD library parts in the IEC 61188-7 rotation.

The proposed IPC-7351C included Level A (current IPC standard) and Level B (IEC standard) component rotations.

The main scope of zero-component orientations was to establish a consistent technique for the description of electronic component orientation, and their land pattern geometries, that facilitates and encourages a common data capture and transfer methodology amongst and between global trading partners.

IPC, in conjunction with the International Electrotechnical Commission (IEC), have established several standards that are in the process of being coordinated. One of the standards is on the design of land patterns geometries (IPC-7351/IPC-7352/IEC 61188-5-1); the other set is on electronic description for data transfer between design and manufacturing (IPC-2581/IEC 61182-2). To maintain a consistent method where these two important standards describe the component mechanical outlines, and their respective mounting platforms, a single concept must be developed that takes into account various factors within the global community.

Many large firms have spent millions of dollars creating and implementing their own unique standards for their own “Electronic Product Development Automation”. These standards are proprietary to each firm and are not openly shared with the rest of the industry. This has resulted in massive duplication of effort costing the industry millions of man hours in waste and creating industry chaos and global non-standardization.

The industry associations responsible for component descriptions and tape and reel orientation have tried valiantly to influence the industry by making good standards that describe the component outlines and how they should be positioned in the delivery system to the equipment on the manufacturing floor. Suppliers of parts have either not adhered to the recommendations or have misunderstood the intent and provided their products in different orientations.

The Land pattern standards put an end to the “Proprietary Intellectual Property” and introduce a world standard so every electronics firm can benefit from Electronic Product

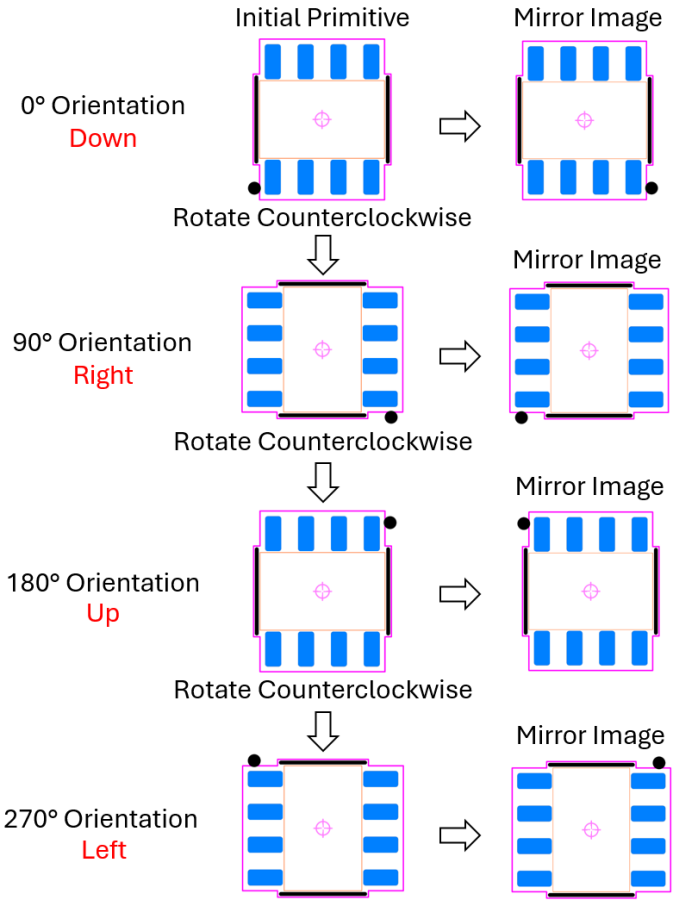
Development Automation. The data format standards (IPC-2581 and IEC 61182-2) are an open database XML software code that is neutral to all the various CAD ASCII formats. For true machine automation to exist, the world desperately needs a neutral CAD database format that all PCB manufacturing machines can read.

The main purpose of creating the land pattern standards is to achieve reliable solder joint formation platforms; the reason for developing the data transfer structure is to improve the efficiency with which engineering intelligence is converted to manufacturing reality. Even if the neutral CAD format can drive all the manufacturing machines, it would be meaningless unless the component description standard for CAD land patterns was implemented with some consistency. Zero Component Orientation has a key role in machine automation.

The obvious choice for global standardization for EE hardware engineering, PCB design layout, manufacturing, assembly and testing processes is to incorporate the standard land pattern conventions. Any other option continues the confusion and additional manual hours of intervention in order to achieve the goals of automation. In addition, the ease of having one system export a file so that another system can accomplish the work may require unnecessary manipulation of the neutral format in order to meet the object of clear, unambiguous software code.

The design of any assembly will continue to permit arrangement and orientation of components at any orientation consistent with design standards. Starting from a commonly understood data capture concept will benefit the entire supply chain.

Here is the flow for zero-component orientation and the counterclockwise rotation of a standard 8-pin SOIC.



# 23.0 – Standard Reference Designators

| | | | |
|---|---|---|---|
| **A** | Separable Assembly | **LS** | Loudspeaker, Buzzer |
| **AR** | Amplifier | **M** | Meter |
| **AT** | Attenuator; Isolator | **MG** | Motor-Generator |
| **B** | Blower, Motor | **MH*** | Mounting Hole |
| **BT** | Battery | **MK** | Microphone |
| **C** | Capacitor | **MP** | Mechanical Part |
| **CB** | Circuit Breaker | **P** | Connector, Plug, Male |
| **CP** | Connector Adapter, Coupling | **PS** | Power Supply |
| **CN** | Capacitor Network | **Q** | Transistor |
| **CR** | Breakdown Diode | **R** | Resistor |
| **D** | Diode | **RN** | Resistor Network |
| **DC** | Directional Coupler | **RT** | Thermistor |
| **DL** | Delay Line | **RV** | Varistor, Variable Resistor |
| **DS** | Display, Lamp | **S** | Switch |
| **E** | Terminal | **T** | Transformer |
| **F** | Fuse | **TB** | Terminal Board, Terminal Strip |
| **FD*** | Fiducial | **TC** | Thermocouple |
| **FL** | Filter | **TP**** | Test Point, In-circuit Test Points |
| **G** | Generator, Oscillator | **TZ** | Transzorb |
| **GN** | General Network | **U** | Inseparable Assembly, IC Pkg. |
| **H** | Hardware | **VR** | Voltage Regulator |
| **HY** | Circulator | **W** | Wire, Cable, Cable Assembly |
| **J** | Connector, Jack, Female | **X** | Fuse holder, Lamp holder, Socket |
| **K** | Contactor, Relay | **Y** | Crystal, Oscillator |
| **L** | Coil, Inductor, Bead, Ferrite Bead | **Z** | Miscellaneous |

*These class letters would not appear in a parts list as they are part of a PCB and not an active electronic component.

**Not a class letter, but commonly used to designate test points for maintenance purposes.

Note: The above list is not exhaustive. See the standard list of class designation letters in ANSI Y32.2/IEEE Standard 315.

# 24.0 – Surface Mount Component Families

## 24.1 – Chips

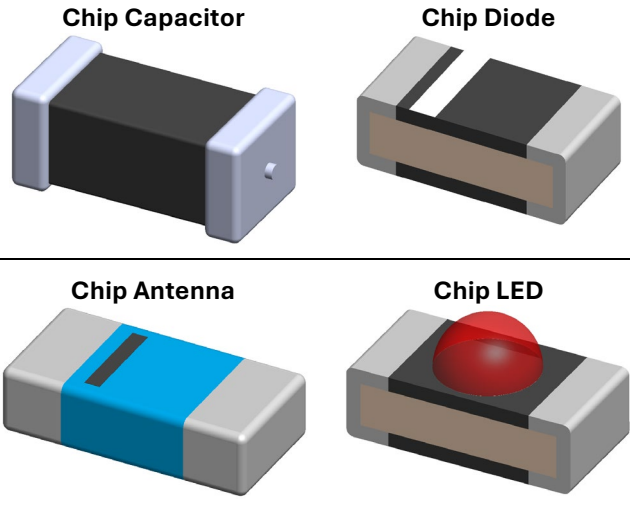
**Chips:** An ultra-compact rectangular housing designed specifically for surface mount discrete passive or semiconductor devices containing exactly two electrical terminals. Electrical contacts are located at opposite ends of the body, wrapping around the edges to form metallized soldering pads. Most 2-pin passive chips are physically symmetrical, allowing automated pick-and-place systems to orient them easily without top-to-bottom or front-to-back errors. The body typically consists of a single block of ceramic (for capacitors), thick-film substrate (for resistors), or molded plastic/glass (for diodes).

**Monolithic Structure:** The body typically consists of a single block of ceramic (for capacitors), thick-film substrate (for resistors), or molded plastic/glass (for diodes).

**Rectangular or Square End-Cap Terminations:** Electrical contacts are located at opposite ends of the body, wrapping around the edges to form metallized soldering pads.

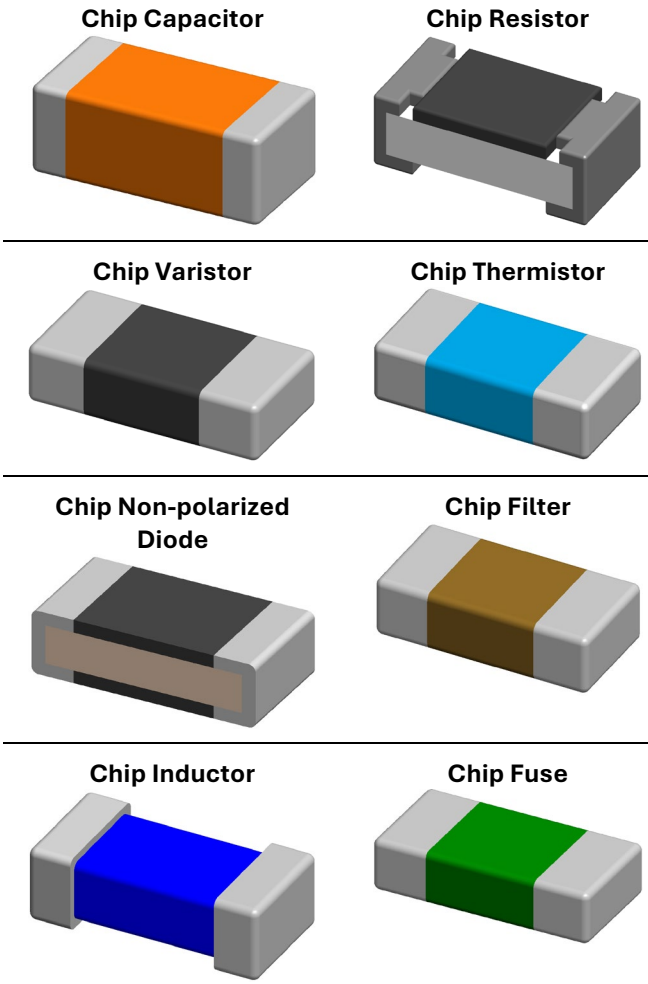
**Symmetrical Design:** Most 2-pin passive chips are physically symmetrical, allowing automated pick-and-place systems to orient them easily without top-to-bottom or front-to-back errors.

**Polarized Chip Packages**




**EIA**: PDP-100

**Non-Polarized Chip Packages**




| Chip Size Codes with Inch Dimensions | |
|---|---|
| **EIA (inch) Name** | **Inch Dimensions** |
| 01005 | 0.0157 in × 0.0079 in |
| 0201 | 0.024 in × 0.012 in |
| 0402 | 0.039 in × 0.020 in |
| 0603 | 0.063 in × 0.031 in |
| 0805 | 0.079 in × 0.049 in |
| 1008 | 0.098 in × 0.079 in |
| 1206 | 0.126 in × 0.063 in |
| 1210 | 0.126 in × 0.098 in |
| 1806 | 0.177 in × 0.063 in |
| 1812 | 0.180 in × 0.130 in |
| 2010 | 0.197 in × 0.098 in |
| 2512 | 0.250 in × 0.130 in |
| 2920 | 0.290 in × 0.200 in |

| Chip Size Codes with Metric Dimensions | |
|---|---|
| **IEC (metric) Name** | **Metric Dimensions** |
| 0402 | 0.40 mm × 0.20 mm |
| 0603 | 0.60 mm × 0.30 mm |
| 1005 | 1.00 mm × 0.50 mm |
| 1608 | 1.60 mm × 0.80 mm |
| 2012 | 2.00 mm × 1.25 mm |
| 2520 | 2.50 mm × 2.00 mm |
| 3216 | 3.20 mm × 1.60 mm |
| 3225 | 3.20 mm × 2.50 mm |
| 4516 | 4.50 mm × 1.60 mm |
| 4532 | 4.50 mm × 3.20 mm |
| 5025 | 5.00 mm × 2.50 mm |
| 6332 | 6.40 mm × 3.20 mm |
| 7451 | 7.40 mm × 5.10 mm |

**Performance & Manufacturing Challenges**

**Tombstoning Risk:** Because these chips have only two terminals, an imbalance in surface tension during solder reflow can cause the component to lift off one pad and stand vertically like a tombstone. This is minimized by maintaining perfectly symmetrical landing pads and thermal reliefs.

**Ultra-Low Parasitics:** The absence of long lead wires reduces parasitic inductance and capacitance, making these packages ideal for high-speed signal integrity and high-frequency RF layouts.

**High-Speed Placement:** Their flat, symmetrical shapes make them highly optimized for automated vacuum pick-and-place nozzles, allowing assembly machines to shoot thousands of these components per minute.

## 24.2 – Molded Body

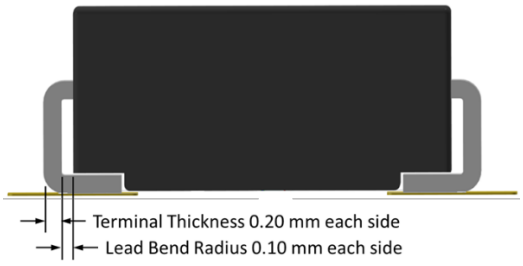
**Molded Body:** Electronic component housings formed by encapsulating internal elements (such as a silicon die, a capacitor element, or a lead frame) in a solid, injection-molded thermoset plastic or epoxy resin. Unlike generic ceramic or open-frame structures, these packages provide an airtight, structurally rigid shield that safeguards components against moisture, physical impact, and operational vibration.

**Inward L-Bend Lead:** The leads curl tightly underneath the molded plastic shell. This saves valuable PCB area, though it hides the solder joints from easy optical inspection.

**Heel and Toe Goals:** IPC guidelines dictate robust calculation values for the Toe (outer edge) and Heel (inner edge) of the pad. These parameters ensure that the solder fillet achieves high mechanical joint strength.

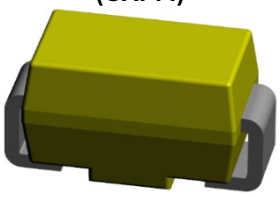
**Side Goal Omission:** For many molded body components – specifically those utilizing Inward L-Bends – IPC standards omit a side-joint goal requirement. Adding extra pad width along the sides does not increase mechanical hold. Furthermore, excess side solder can cause the component to float or rotate out of alignment during the reflow oven cycle.

**3D STEP Model:** in order to get an accurate 3D STEP model, the outside Terminal span dimension 'D' must be 0.60 mm less than the body length 'D1' dimension to allow space for the terminal lead to exit the package body and the terminal lead bend and terminal lead 0.20 thickness on both sides.

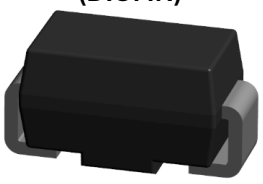



**Non-Polarized**
**Molded Body Inward Flat Ribbon Components**

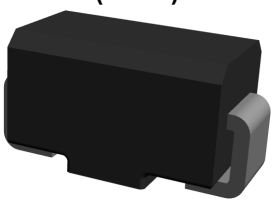
**Molded Capacitors (CAPM)**



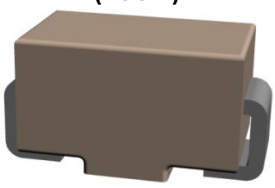
**Molded Diode (DIOMN)**



**Molded Body Inductor (INDM)**

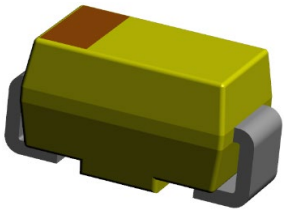


**Molded Fuses (FUSM)**

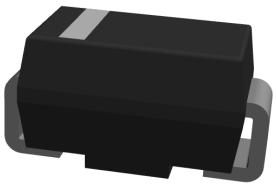


**Polarized**
**Molded Body Inward Flat Ribbon Components**

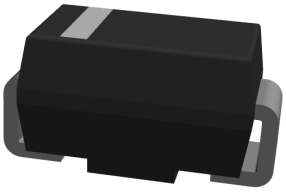
**Capacitor (CAPPM)**



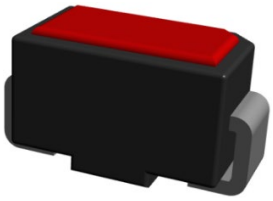
**Molded Body Diode (DIOM)**



**Molded Inductor (INDPM)**



**Molded Body LED (LEDM)**



**JEDEC**: DO-214

| Common Molded Body Tantalum Capacitors | | | |
|---|---|---|---|
| **EIA Size Code** | **Package Dimensions** | **KEMET Code** | **AVX Code** |
| 2012-12 | 2.00 x 1.30 x 1.20 | R | R |
| 3216-10 | 3.20 x 1.60 x 1.00 | I | K |
| 3216-12 | 3.20 x 1.60 x 1.20 | S | S |
| 3216-18 | 3.20 x 1.60 x 1.80 | A | A |
| 3528-12 | 3.50 x 2.80 x 1.20 | T | T |
| 3528-21 | 3.50 x 2.80 x 2.10 | B | B |
| 6032-15 | 6.00 x 3.20 x 1.50 | U | W |
| 6032-28 | 6.00 x 3.20 x 2.80 | C | C |
| 7260-38 | 7.30 x 6.00 x 3.80 | E | V |
| 7343-20 | 7.30 x 4.30 x 2.00 | V | Y |
| 7343-31 | 7.30 x 4.30 x 3.10 | D | D |
| 7343-43 | 7.30 x 4.30 x 4.30 | X | E |

**Key Physical Features**

- **Fully Encapsulated Core:** Thermoset epoxy compound forms a solid protective layer on all sides, completely insulating the sensitive inner structures (such as silicon dies, wound wires, or sintered tantalum pellets) from environmental elements.
- **Integrated Polarity Markers:** Because the body is formed in an injection-molding process, bevels, chamfered corner notches, or deep laser-etched bands are built directly into the plastic to indicate polarity (essential for diodes and tantalum caps).
- **Wrap-Around or Inward Terminations:** Leads typically exit the bottom or centerline of the plastic molding and are bent flat against the body ends or tucked flush as leadless bottom contacts.
- **Classifications & Examples:** Molded body packages use unique design rules and prefixes to accurately map their footprint requirements.

**Tantalum Capacitors** (CAPMP / EIA Standard): Features highly standardized molded packages categorized by standard uppercase lettering.

- A Case (3216 Metric): 3.20 mm x 1.60 mm nominal
- B Case (3528 Metric): 3.50 mm x 2.80 mm nominal
- C Case (6032 Metric): 6.00 mm x 3.20 mm nominal
- D Case (7343 Metric): 7.30 mm x 4.30 mm nominal

**Diodes** (DIOM / JEDEC DO-214): Molded discrete diodes leverage robust, wide wrap-around terminal feet built to absorb thermal stress.

- SMA (DO-214AC): Smallest common molded diode variant
- SMB (DO-214AA): Medium profile option
- SMC (DO-214AB): Largest footprint format supporting high power surge ratings

**Engineering Design Parameters:** When laying out a land pattern for a molded body part with Footprint Expert use distinct math models.

- **Molded Body Side Goal:** Footprint generation tools use a unique variable known as the "Molded Body Side Goal" to ensure the copper landing pads extend far enough beyond the side boundaries of the plastic block, keeping the solder joint from bridging or starving.
- **Heel Fillet Compensation (Jh):** Because molded leads often tuck close or underneath the plastic shell, the heel fillet calculations must account for package chamfering to prevent cold solder joints or component tilt.
- **Robust Placement Courtyard:** Since the molding process can incur minor edge tolerances (+/-0.2 mm package deviations), the IPC placement courtyard boundary must be generous enough to account for physical variations during automated assembly pick-and-place tracking.

**Performance Advantages**

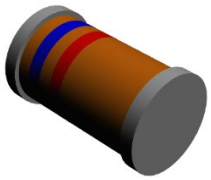
- **High Moisture Resistance:** Direct plastic encapsulation eliminates internal air pockets, effectively blocking moisture ingress and saving parts from internal corrosion or short circuits.
- **Structural Resistance to Shock:** The solid core cushions internal components from physical drops, heavy vibrations, and handling damage during rapid assembly lines.

- **Perfect Coplanarity Control:** Flat molded bottoms provide a highly stable seating plane during reflow, significantly reducing defects like skewing or uneven floating.
- **Cost Efficiency:** Plastic transfer molding remains the most affordable, mass-producible chip encapsulation method in modern electronics manufacturing

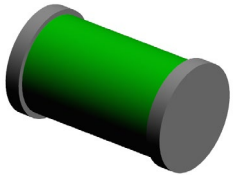
## 24.3 – Metal Electrode Leadless Face (MELF)

**Metal Electrode Leadless Face (MELF):** A specialized surface mount component package characterized by a cylindrical body with metallized round end caps. Unlike standard rectangular chip components, MELF packages are round and do not use traditional leads. They are primarily used for high-reliability resistors, fuses and diodes where superior thermal stability, low noise, and excellent moisture resistance are required.

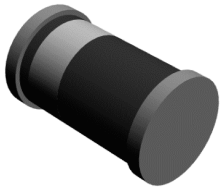
**MELF Resistor (RESMELF)**



**MELF Fuse (FUSEMELF)**



**MELF Diode (DIOMELF)**



**JEDEC**: DO-213

**Cylindrical Body:** The housing is a glass or ceramic tube, making it highly resistant to thermal shock and moisture

**Leadless Endcaps:** Metal caps wrap around the circular edges on both ends, serving as the soldering terminals.

**No Orientation Issues:** Because it is perfectly round, the component can rotate along its long axis during placement without affecting its electrical connection.

**Superior Reliability:** MELF components offer exceptionally low failure rates and excellent long-term stability under harsh conditions.

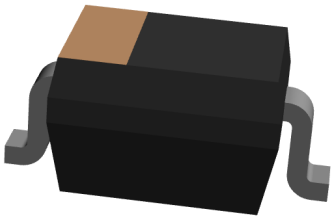
**High Thermal & Power Handling:** The cylindrical shape provides a larger surface area than flat chips, allowing better heat dissipation and higher power ratings.

**Low Noise & Parasitic:** Excellent for high-frequency or high-precision circuits due to minimal structural inductance and capacitance.

| Common MELF Package Sizes | | |
|---|---|---|
| **Common Case Names** | **Size Code** | **Package Dimensions** |
| MicroMelf (MMU) | 0102 | 2.20 L x 1.10 Dia. |
| MiniMelf (MMA) | 0204 | 3.60 L x 1.40 Dia. |
| Melf (MMB) | 0207 | 5.80 L x 2.20 Dia. |

## 24.4 – Small Outline Diode (SOD) with Gullwing Leads

**Small Outline Diode (SOD) with Gullwing Leads:** A standard surface mount semiconductor package designed for discrete components like switching, Schottky, and Zener diodes.



**JEDEC**: DO-215

**Lead Design:** The "Gullwing" description means the metal leads bent downward and then outward.

**Soldering & Assembly:** These leads provide solid footing on the copper pads during assembly. They are ideal for automated pick-and-place and reflow soldering but are also large enough to allow for relatively easy hand soldering.

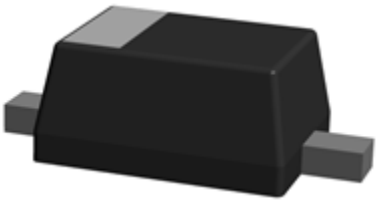
**Package Variants:** This package style comes in various standardized sizes to accommodate different thermal requirements and spatial limitations.

**Common Applications Include:** Smartphones and wearable devices, IoT modules and compact consumer electronics, Power supply circuits and automotive modules, LED lighting drivers and signal conditioning.

| Common Small Outline Diode (SOD) Sizes | |
|---|---|
| **Case Code** | **Package Dimensions** |
| SOD-123 | 3.68 mm x 1.17 mm x 1.60 mm |
| SOD-128 | 5.00 mm x 2.70 mm x 1.10 mm |
| SOD-323 | 1.70 mm x 1.25 mm x 0.95 mm |
| SOD-523 | 1.25 mm x 0.85 mm x 0.65 mm |
| SOD-723 | 1.40 mm x 0.60 mm x 0.59 mm |

## 24.5 – Small Outline Diode Flat Lead (SODFL)

**Small Outline Diode Flat Lead (SODFL):** A compact, ultra-low-profile surface mount technology (SMT) semiconductor housing designed to replace standard Gullwing SOD packages. By utilizing flat, folded metal ribbons that lie completely flush beneath the bottom of the device rather than curve outward, it maximizes board space, increases power handling, and significantly lowers the component profile.



**JEDEC**: DO-219, DO-221, DO-222

**Core Advantages Over Gullwing Variants:**

- **Space Saving:** Eliminating extending Gullwing leads shrinks the necessary circuit board footprint. For example, an SOD-123FL serves as a direct drop-in replacement on existing pads but reduces physical component clearance.
- **Superior Thermal Performance:** Because the flat leads are positioned directly underneath the component body, the heat dissipation path to the PCB copper pads is incredibly short. This design offers up to 25% lower thermal resistance compared to standard packages.
- **Ultra-Low Profile:** These packages typically feature a maximum height profile of just 1.00 mm to 1.20 mm. This represents a profile reduction of 25% or more compared to traditional alternatives, making them ideal for high-density stack-ups.
- **Increased Surge Capacity:** Many flat lead designs incorporate an internal clip-attach structure rather than fragile wire bonds. This structural change boosts transient forward surge-current survival.

**Common Applications:** The combination of enhanced thermal dissipation and minimized Z-axis height makes SODFL variants highly desirable for:

- **Portable Electronics:** Ultra-thin smartphones, smartwatches, and portable power banks.
- **Power Conversion:** Secondary rectification and freewheeling diodes in compact AC/DC or DC/DC converters.
- **Circuit Protection:** High-efficiency Schottky rectifiers, Zener voltage stabilizers, and Transient Voltage Suppression (TVS) applications.

## 24.6 – Capacitor, Aluminum Electrolytic (CAPAE)

**Capacitor, Aluminum Electrolytic (CAPAE):** A specialized housing used for components that provide high volumetric capacitance in a relatively compact space. Constructed by winding an anode foil, paper separators saturated with liquid electrolyte, and a cathode foil into a cylinder, these packages are polarized and feature distinct physical markers to indicate the negative terminal.

**IEC**: 60384-26

Unlike monolithic ceramic capacitors, these parts are housed in distinct mechanical form factors dictated by their mounting style, ripple current capability, and spatial constraints.

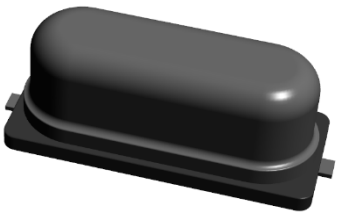
SMD aluminum electrolytic capacitors are typically packaged in cylindrical metallic aluminum "cans" sitting atop a square, black plastic insulating base. The base bends the terminal leads flat under the component body to create solder pads for reflow soldering.

**Polarity Indicator:** A highly visible black or dark colored crescent/stripe painted directly onto the top face of the metallic cylinder denotes the negative pad.

| Common Aluminum Electrolytic Capacitor Sizes | | |
|---|---|---|
| **Case Code** | **Diameter x Height** | **Common Values** |
| A | 4.00 mm x 5.40 mm | 1uF to 10uF (50V) |
| B | 5.00 mm x 5.40 mm | 10uF to 22uF (35V) |
| C | 6.30 mm x 5.40 mm | 47uF to 100uF (16V) |
| D | 6.30 mm x 7.70 mm | 100uF to 22uF (25V) |
| F | 8.00 mm x 10.20 mm | 220uF to 470uF (35V) |
| G | 10.0 mm x 10.20 mm | 470uF to 1000uF (16V) |

## 24.7 – Crystals (XTAL)

**Crystals (XTAL):** A specialized, surface mount housing designed for passive timing components. Unlike multi-pin active oscillators that require separate power, a 2-pin crystal package only contains the raw quartz blank and two electrical terminals. It relies entirely on the microcontroller's internal inverter circuit to generate a clock signal.



**Construction and Hermetic Sealing:** Because quartz crystals are highly sensitive to moisture, dust, and atmospheric pressure changes, the packages utilize a hermetic (airtight) seal.

- **The Body:** The base is typically constructed from a multi-layer technical ceramic material.
- **The Lid:** A metal seam-welded lid or a glass-sealed ceramic lid covers the top. This metal lid is often grounded internally or externally to shield the sensitive crystal blank from Electromagnetic Interference.

SMD crystal packages are standardized by their physical length and width dimensions. The industry has shifted heavily toward smaller footprints to fit dense modern electronics.

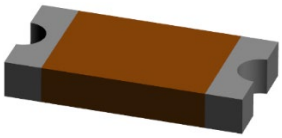
| Common SMD Crystal Packages | | |
|---|---|---|
| **Case Code** | **Package Dimensions L x W x H Range** | **Typical Uses** |
| 5032 | 5.0 x 3.2 x 1.0 -1.20 mm | Microcontrollers |
| 3225 | 3.2 x 2.5 x 0.7 - 0.90 mm | Ease of Routing |
| 2520 | 2.5 x 2.0 x 0.5 - 0.60 mm | loT Modules |
| 2016 | 2.0 x 1.6 x 0.45 mm | Smartphones |

## 24.8 – Side Concave Packages 2-pin

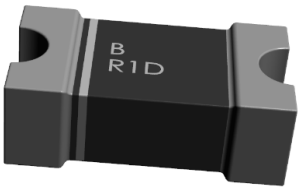
**Side Concave Packages:** A surface mount electronic component housing where the electrical terminations or leads are recessed into indented, semicircular, or "scalloped" channels along the vertical sidewalls of the component body. Unlike standard convex component packages where leads protrude outward (like Gullwing leads) or flat surfaces, the concave architecture places the solderable terminals inside these inner grooves.

**Side Concave Crystal**

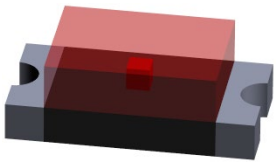
**Side Concave Inductor**



**Side Concave Diode**




**Side Concave LED**



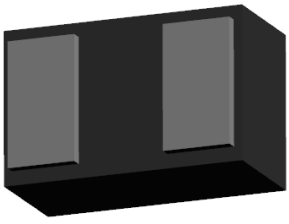
**Assembly and Manufacturing Impact**

- **Solder Joint Integrity:** Early designs favored concave configurations under the assumption that isolating the paste within the inner channel would mitigate solder bridging. Modern automated optical inspection (AOI) data shows that the absolute spacing on the PCB pad layout dictates bridging protection far more than the concave shape itself.
- **No-Lead Visual Inspection:** Certain modern variations of side concave packages overlap with side-wettable flanks seen in Dual Flat No-Lead (DFN) configurations. This recess allows solder paste to travel upward into the side groove, creating a visible fillet that validates a solid mechanical bond during high-speed assembly inspection.

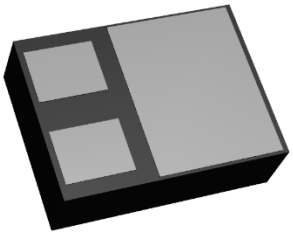
## 24.9 – Dual Flat No-Lead (DFN)

**Dual Flat No-Lead (DFN):** A surface mount electronic component housing with a near-zero profile that replaces traditional extending leads with flat, metal contact pads on its underside.

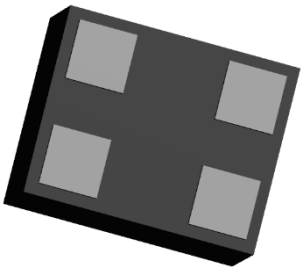
**DFN 2-Pin Diode & LED**



**DFN 3-Pin Transistor**



**DFN 4-Pin Oscillator**



**JEDEC**: MO-236. TO-276

**Key Design and Structural Features**

- **Bottom-Surface Pads:** Electrical contacts sit flush with the bottom plastic mold compound, eliminating vulnerable, bendable pins.
- **Thermal Pad:** Most DFN packages feature an exposed center metal pad that is soldered directly to the PCB to channel heat away from the silicon die.
- **Ultra-Low Profile:** The compact design minimizes component height and weight, making it ideal for mobile devices and high-density boards.

**Performance Advantages**

- **Excellent Thermal Dissipation:** The exposed center pad creates a direct thermal highway, allowing high power processing in a tiny footprint.
- **Low Parasitic Impedance:** Eliminating long lead wires reduces internal resistance and inductance, enhancing high-frequency signal performance.
- **Cost-Efficient:** The simplified lead frame design uses less raw material and is highly cost-effective to manufacture at scale.

**Assembly and Inspection Challenges**

- **Hidden Solder Joints:** Because the connections sit underneath the package, traditional visual inspection cannot verify electrical connectivity or find voids.
- **Side-Wettable Flanks (SWF):** Modern DFN variants feature a specialized cut or plating on the side edge of the pad. This allows solder to wick up the outer wall, creating a visible fillet for Automated Optical Inspection (AOI).
- **Solder Mask and Stencil Design:** Precise stencil opening design is required for the thermal pad to prevent "floating," where excess solder lifts the component and prevents the perimeter signal pads from making contact.

## 24.10 – Small Outline Transistor SOT23 (SOT Form Factor)

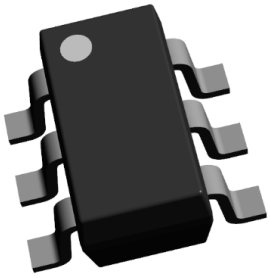
**Small Outline Transistor SOT23 (SOT Form Factor):** A highly popular, compact, plastic-molded surface mount device (SMD) package. Widely used for diodes, BJT transistors, MOSFETs, and voltage regulators, it features Gullwing leads extending from its two long sides and is favored for its space efficiency in modern electronics. Typically, 3 pins, though 5-pin (SOT23-5) and 6-pin (SOT23-6) variants are heavily used for small logic ICs and operational amplifiers. Because SOT-23 packages lack a dedicated thermal pad underneath, heat must be dissipated through the copper traces on the PCB. To optimize cooling, expand the copper connected to the pins (particularly the wider drain or collector pin).

| Gullwing SOT23 Type Form Factor Component Families | | | |
|---|---|---|---|
| **EIA** | **JEITA** | **Pin Pitch** | **Pin Qty** |
| SOT23-3 | SC59 | 0.95 | 3 |
| SOT28 | SC70-8 | 0.65 | 8 |
| SOT323 | SC70 | 0.65 | 3 |
| SOT346 | SC59A | 0.95 | 3 |
| SOT353 | SC88A | 0.65 | 5 |
| SOT363 | SC88 | 0.65 | 6 |
| SOT416 | SC75 | 0.50 | 3 |
| SOT753 | SC74A | 0.95 | 5 |

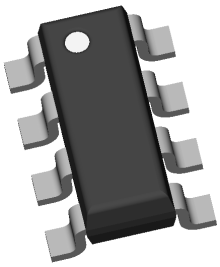
**SOT23-3**

**SOT23-5**

**SOT23-6**



**SOT23-8**

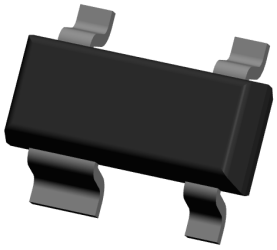


**JEDEC**: TO-236
(SOT23-5): MO-178
(SOT23-6): MO-193

## 24.11 – Small Outline Transistor SOT143 (SOT)

**Small Outline Transistor SOT143 (SOT):** A low-profile, plastic surface mount package featuring four Gullwing leads. Derived directly from the standard SOT-23 geometry, it is uniquely characterized by having one lead that is visibly wider than the other three. This asymmetrical pin layout enforces a built-in reverse-polarity protection, making it a staple for high-frequency radio frequency (RF) transistors, Schottky/PIN diodes, TVS protection arrays, and voltage supervisor circuits.

**SOT143**



**SOT143 Reverse**

**JEDEC**: TO-253, TO-261

**PCB Design & Footprint Guidelines**

- **Orientation Verification:** Because of the asymmetrical fourth lead, CAD footprint library creation must map exactly to the manufacturer's pinout. The wider pad acts as an un-cloneable indicator for automatic vision-inspection and pick-and-place indexing.
- **RF Grounding & Thermal Benefits:** The broadened lead is not just a layout guide; it dramatically drops package inductance. This provides an exceptionally clean ground path for RF designs. Furthermore, it serves as the package's primary thermal conduit to the board, so pulling a substantial copper pour out from this wide pad is recommended.
- **Solder Bridging Risk:** Although the side-to-side pitch is spacious, the end-to-end clearance requires exact solder mask dam tracking to prevent solder bridging across the small gaps

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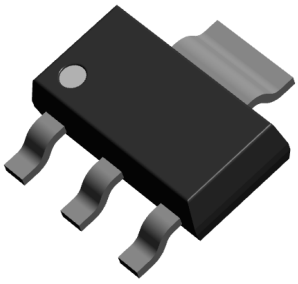
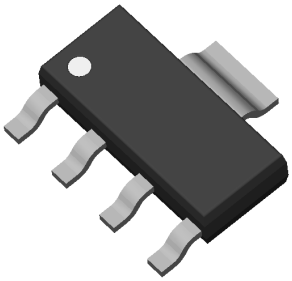
## 24.12 – Small Outline Transistor SOT223 (SOT)

**Small Outline Transistor SOT223 (SOT):** A medium-power, plastic surface mount device package. It is widely chosen for discrete semiconductors and integrated circuits that require robust thermal handling in a compact layout, such as linear voltage regulators, power MOSFETs, and load switches.

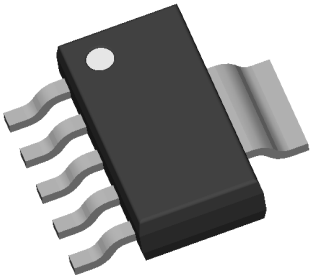
**SOT223-4**



**SOT223-5**



**SOT223-6**



**JEDEC**: TO-261

**Key Physical Characteristics**

- **Lead Configuration:** It typically features four leads total: three standard Gullwing pins on one side of the body and one large, exposed tab on the opposite side.
- **The Thermal Tab:** The large tab is mechanically and electrically continuous with the center pin (Pin 2). It provides a direct, low-resistance thermal path to conduct heat away from the silicon die into the PCB.
- **Body Dimensions:** The main plastic body measures roughly 6.50 mm x 3.50 mm with an overall profile height of 1.65 mm. Including the leads, the total width span is approximately 7.00 mm.
- **Pin Pitch:** The distance between the centers of the three adjacent pins is 2.30 mm for 4-pin and 1.50 mm for 5-pin and 1.27 for 6-pin.

**PCB Footprint & Layout Guidelines**

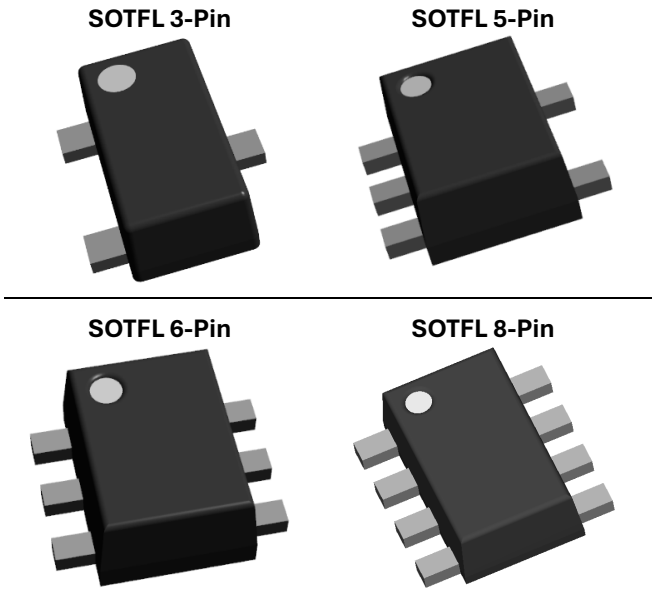
- **Thermal Management & Copper Pour:** Because the package dissipates more power than smaller standard packages like the SOT-23, its performance relies heavily on your PCB layout.
  - Connect a large copper pour directly to the pad of the large thermal tab.
  - Drop a matrix of thermal vias into the tab pad to transfer heat to internal or bottom-side ground/power planes. Without adequate copper area, the component will overheat and trigger thermal throttling or fail prematurely.
- **Electrical Isolation Considerations:** The large tab is typically tied to a specific net (often Vout or GND),

depending on the component). Ensure that neighboring signal traces or component pads maintain safe electrical clearance from the enlarged copper pour surrounding this tab pad.

- **Soldering and Solder Mask:** Because the pin pitch is a relatively wide 2.30 mm, the package is highly forgiving for both automated assembly line reflow ovens and manual prototyping hand-soldering. However, ensure your footprint includes a precise solder mask cutout for the thermal tab to prevent solder pooling from shifting the smaller pins out of alignment during reflow.

## 24.13 – Small Outline Flat Lead (SOFL)

**Small Outline Flat Lead (SOFL):** A surface mount integrated circuit (IC) package characterized by a low-profile rectangular body and flat, non-extended leads rather than standard protruding Gullwing pins. It bridges the gap between traditional small outline packages (SOP/SOIC) and bottom-termination flat packs, providing a space-efficient layout tailored for tight vertical clearances and high-frequency, automated PCB assembly.




**JEDEC**: MO-293

**Key Physical Features**

- **Flat Lead Structure:** The leads do not wrap or form distinct Gullwings. They lie flush against the underside or periphery of the device, which minimizes parasite inductance.
- **Dual-Sided Orientation:** Pins or landing pads typically extend along two opposite sides of the rectangular body.
- **Low Profile:** The "Flat" designation prioritizes a thin z-axis height, perfect for tight enclosures like laptops, memory modules, and portable smart devices.
- **Exposed Thermal Pad (Often Included):** Many variations incorporate an internal die attach paddle exposed on the bottom side. This pad solders directly to the PCB to conduct heat away efficiently.

**Design Parameters**

When creating an IPC-7351 standardized land pattern for an SOFL package, engineers focus on several specific features:

- **Pitch:** Typically ranges between 0.50 mm to 1.00 mm depending on the subcategory variant.
- **Pads:** Footprints require flat, rectangular SMD copper pads.
- **Solder Mask:** Non-Solder Mask Defined (NSMD) pads are preferred to guarantee high registration accuracy.
-

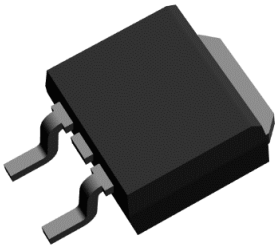
**Performance Advantages**

- **High Signal Integrity:** Shorter, flatter leads drastically lower parasitic capacitance and inductance, making them superior for high-speed switching applications.
- **Excellent Heat Dissipation:** Direct bottom-pad soldering turns the PCB's ground planes into large heat sinks via thermal vias.
- **Space Efficiency:** Frees up vertical height and tighter pitch allows dense layout clustering.

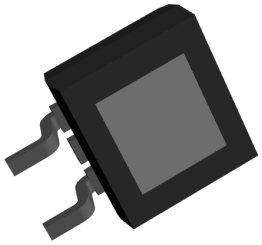
## 24.14 – DPAK

**DPAK:** A standard surface mount transistor package designed for high-power semiconductor devices. It features a large metal tab that solders directly to the PCB to dissipate heat. It is widely used for voltage regulators, MOSFETs, and power diodes.

**DPAK Extended Thermal Tab**



**DPAK Under Body Thermal Tab**



**JEDEC**:
MO-169, MO-235, MO-306, TO-251, TO-252, TO-268

**Key Physical Features**

- **Thermal Tab**: A large metal backside tab acting as the primary drain/collector connection and heat sink.
- **Three-Terminal Layout**: Typically features two smaller leads and one large clipped lead or tab.
- **Surface Mount Design**: Eliminates the need for through-holes, speeding up automated assembly.

**Design Parameters**

- **Lead Pitch**: Standard distance between the smaller pins is 2.30 mm (0.090 inches).
- **Thermal Vias**: Footprints require an array of vias under the tab to transfer heat to internal copper layers.
- **Solder Paste Stencil**: The large tab pad requires a windowpane stencil pattern to prevent component floating and solder splattering.

**Performance Advantages**

- **High Power Handling**: Safely manages higher currents and voltages than standard small-outline packages.
- **Low Thermal Resistance**: Direct copper-to-copper bonding ensures rapid heat transfer away from the silicon die.
- **Robust Mechanics**: The large soldered surface area provides high mechanical stability against vibration.

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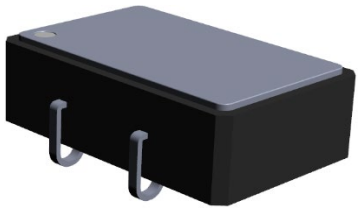
## 24.15 – Oscillator, J-Lead (OSCJ)

**Oscillator, J-Lead (OSCJ):** A surface mount, plastic-molded enclosure specifically designed for crystal oscillators, clock generators, and frequency control devices. It adapts the traditional Small Outline J-Lead (SOJ) format into a 4-pin or 6-pin specialized housing, featuring pins that curl downward and inward beneath the device body resembling the letter "J". This configuration provides an alternative to standard leadless ceramic packages (LCC) by adding robust mechanical flexing capabilities to critical timing circuits.



**Key Physical Features**

- **Inward-Curled J-Leads:** Unlike protruding Gullwing leads that extend outward, J-leads tuck directly under the plastic body. This structural choice saves significant board real estate over standard SOIC components.
- **Plastic Molded Body:** Typically features a rugged, molded plastic encapsulation housing the quartz crystal blank and its active oscillation IC circuitry.
- **Standardized Pinouts:** Usually configured as a 4-pin or 6-pin module. In a standard 4-pin configuration, the pinouts follow this layout:
  - Pin 1: Tri-State Enable/Disable or No Connect
  - Pin 2: Ground (GND)
  - Pin 3: Output Frequency Clock
  - Pin 4: Supply Voltage (VDD)

**Design Parameters**

When laying out a land pattern for an OSCJ component on a board, designers prioritize the following IPC-compliant geometries:

- **Footprint Pads:** The copper pads must extend slightly outward and inward relative to the J-lead apex to guarantee a proper solder fillet formation along both the inner and outer curve of the lead.
- **Pitch:** Large-form plastic OSCJ packages typically leverage a generous lead pitch, commonly at 2.54 mm or 5.08 mm, ensuring high electrical isolation between high-frequency outputs and supply traces.

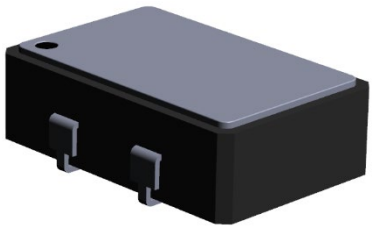
- **Common Dimensions:** These packages are usually larger than modern ceramic variants, with a popular historical standard footprint measuring roughly 14.00 mm x 9.8 mm.

**Performance Advantages**

- **Thermal & Shock Compliance:** The J-lead structure functions like a miniature spring. This flexibility absorbs mechanical shock, vibration, and Coefficient of Thermal Expansion (CTE) mismatches better than rigid, leadless ceramic packaging.
- **Solder Joint Visual Inspection:** Because the J-lead curls along the outer side of the body, the solder heel and toe fillets remain visibly accessible for automated optical inspection (AOI).
- **High Pre-Solder Resiliency:** The tucked lead geometry keeps the component leads protected from accidental bending or misalignment during shipping, tape-and-reel feeding, or handling prior to reflow.

## 24.16 – Oscillator, L-Lead (OSCL)

**Oscillator, L-Lead (OSCL):** A surface mount enclosure designed for quartz crystal oscillators and clock generators. It features L-shaped leads that extend outward and bend downward to form a flat seating plane flush with the PCB surface. This geometry mimics a standard Gullwing style but is specialized for the weight, height, and frequency constraints of surface mount timing modules.



**Key Physical Features**

- **Outward-Extended L-Leads:** Leads protrude from the sides of the package and bend downward and outward, forming an "L" shape.
- **Highly Visible Solder Fillets:** The extended foot of the "L" lead sits entirely outside the component body outline, allowing for straightforward automated visual inspection.
- **4-Pin or 6-Pin Layout:** Typically follows standard oscillator pin configurations (VDD), Ground, Output, and Enable/Disable).

**Design Parameters**

- **Footprint Pad Extension:** Land patterns require a longer pad length extending beyond the lead tip (toe) to ensure a strong solder fillet.
- **Pitch Standards:** Typically features a standard pitch of 2.54 mm or 1.27 mm for robust isolation of high-frequency clock signals.
- **Coplanarity:** Requires strict lead coplanarity tolerance (usually within 0.10 mm) to ensure all L-feet sit perfectly flat on the solder paste during reflow.

**Performance Advantages**

- **Superior Solder Joint Inspection:** Unlike leadless (LCC) or J-lead variants, the entire solder joint is fully visible from above, making it highly compatible with basic Automated Optical Inspection (AOI) systems.
- **Excellent Mechanical Reworkability:** The exposed outward leads make it one of the easiest oscillator packages to rework, manually desolder, or probe during debugging.
- **Stress Relief:** The bend in the L-lead provides mild compliance, absorbing physical board flex and thermal expansion stresses better than leadless ceramic packages.

## 24.17 – Oscillator, Corner Concave (OSCCC)

**Oscillator, Corner Concave (OSCCC):** A standardized, surface mount ceramic or plastic packaging format designed specifically for highly miniaturized crystal oscillators and clock generators. Rather than using extended metal leads like J-leads or Gullwing pins, an OSCCC package utilizes castellated solder pads recessed directly into the vertical corners of the component's body. This design maximizes component density on dense circuit boards while ensuring robust high-frequency electrical isolation.

**Key Physical Features**

- **Corner Castellations (Concave Terminals):** Solder contacts form semi-cylindrical metallized grooves or scallops on the outermost four corners of the device. Solder wicks up these inner vertical channels during reflow.
- **Leadless Profile:** The total absence of outward-extending leads eliminates risk of bent pins, ensuring a completely flat bottom seating plane.
- **Hermetically Sealed Body:** Usually constructed with a ceramic substrate capped by a metal lid to insulate the sensitive internal quartz resonator or MEMS core from atmospheric moisture and environmental aging.
- **Standard 4-Pin Output:** The classic corner configuration natively routes the standard 4-pin functional diagram:
  - **Corner 1:** Tri-state Control / Enable / No Connect
  - **Corner 2:** Ground (GND)
  - **Corner 3:** Frequency Output Clock Signal
  - **Corner 4:** Supply Voltage (Vpp)
- **Pad Geometry:** PCB landing pads are placed directly underneath each corner. They must extend slightly outward beyond the component perimeter to accommodate the side solder fillet.
- **Silkscreen Expansion:** Because the metal pads occupy the actual corners of the rectangular body, layout engineers must provide an expanded or modified silkscreen outline to ensure the component outline remains visible during manual inspection.
- **Pin 1 Indicator:** Due to tightly packed corner spaces, standard circular silkscreen dots may conflict with the copper pads; specialized footprint rules apply to shift the Pin 1 indicator clear of the solder joints.

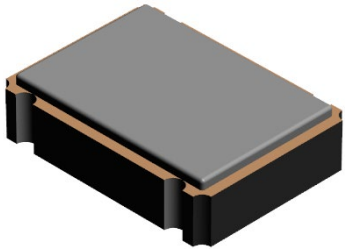
**Performance Advantages**

- **Ultra-Low Parasitic Inductance:** The direct corner contact pathway eliminates the inductive loop area inherent to long J-leads or L-leads, preserving signal integrity for high-speed GHz-range clock signals.
- **Excellent Solder Fillet Inspection:** Because the metallized contact curves up the vertical outer corner edge, inspection cameras can verify a robust, shiny solder joint heel from the side via Automated Optical Inspection (AOI).
- **Maximum Density Space Savings:** Features one of the smallest package envelopes available for clock circuits, saving substantial PCB space compared to plastic-molded leaded components.
- **Self-Alignment:** Surface tension from the molten solder paste pulls the corner cutouts uniformly onto the target footprints during reflow oven cycles, minimizing skewing or rotational placement errors

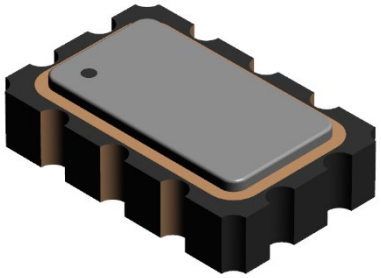
## 24.18 – Oscillator, Side Concave (OSCSC)

**Oscillator, Side Concave (OSCSC):** A standardized, surface mount ceramic or plastic packaging format for quartz crystal oscillators and clock generators. It features castellated solder pads recessed into the flat side edges of the component's body rather than the corners. This design offers a compact, leadless layout that optimizes trace routing and signal path isolation.

**Oscillator Side Concave 4-Pin**



**Oscillator Side Concave 6-Pin**



**Key Physical Features**

- **Side Castellations (Concave Terminals):** Semi-cylindrical, metallized grooves are located along the long or short side edges of the rectangular housing. Solder wicks up these inner vertical channels during reflow.
- **Leadless Profile:** The absence of protruding metal pins eliminates the risk of bent leads, providing a completely flat underside seating plane.
- **Hermetically Sealed Substrate:** Constructed with a rugged ceramic body and a metal lid to protect the internal quartz or MEMS resonator from mechanical stress and moisture.

**IPC Footprint & Design Parameters**

According to IPC-7351B package standards, the naming format follows OSCSC + Length × Width × Height – Pin Count:

- **Pad Geometry:** PCB land pads are positioned flush with the side walls of the oscillator. Pads must extend outward slightly past the package edge to allow a visible side solder fillet to form.
- **Signal Isolation:** Placing pads on the sides keeps the component corners clear, allowing routing traces or ground shield fills to pass cleanly around the corners of the component body.
- **Pin 1 Orientation:** Because the pads sit mid-side, the package corners are ideal for clear silkscreen dots or chamfered edges to mark Pin 1.

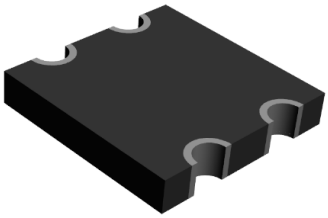
**Performance Advantages**

- **Minimized Parasitic Inductance:** Short, leadless contact paths minimize inductive loops, ensuring stable performance for high-frequency clock signals.
- **Side-Fillet Optical Inspection:** Solder wicks into the side concave channels, allowing easy verification of a robust joint via Automated Optical Inspection (AOI).
- **Self-Alignment:** Surface tension from molten solder draws the side castellations symmetrically onto the PCB land pads, reducing component rotation or shifting during reflow.
- **Board Space Efficiency:** Offers a very tight, low-profile footprint ideal for dense hardware layouts like telecommunication modules, networking cards, and single-board computers.

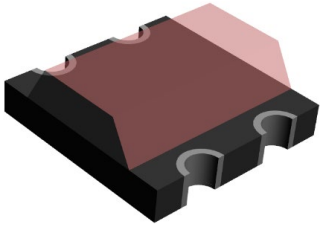
## 24.19 – Side Concave (4-Pin) Diode and LED

**Side Concave (4-Pin) Diode and LED:** A specialized, leadless surface mount footprint standard defined by IPC-7351. Instead of utilizing standard peripheral leads or bottom pads, this package features four metallized semi-cylindrical cutouts (castellated grooves) recessed symmetrically into the side walls of its ceramic or epoxy body. It is primarily implemented for multi-diode arrays and multi-color RGB LEDs, where vertical board profile, trace isolation, and optical inspection are paramount.

**Diode Side Concave 4-Pin**



**LED Side Concave 4-Pin**



**Key Physical Features**

- **Side-Wall Castellations:** The electrical contacts curve upward along the vertical perimeter, creating a concave indentation on the left and right sides.
- **Low-Profile Leadless Structure:** Eliminating outward-facing pins lowers the package clearance, saving surface space and preventing accidental lead bending or damage during automatic component picking.
- **Polarized Geometries:** Components utilize an uneven chamfered corner, a molded notch, or an offset keyway pin configuration to denote diode cathode placement and prevent reverse assembly orientation.

**Common Electrical Configurations**

Because this package format breakout provides four distinct terminal points, it typically services two component families:

- **Multi-Color (RGB) LEDs:** Houses a shared internal node alongside separate color dies. Semicustom variants break out as either a Common Anode configuration (one positive terminal, three separate color cathodes) or a Common Cathode configuration.
- **Integrated Diode Bridges / Arrays:** Integrates a series of four independent rectifier diodes or protection Zeners mapped in a single network (e.g., standard full-wave bridge rectifier or multi-channel ESD clamping array).

**Footprint & PCB Layout Parameters**

When defining this component footprint inside CAD suites like Altium Designer or IPC Footprint Expert, engineering rules mandate precise layout specs:

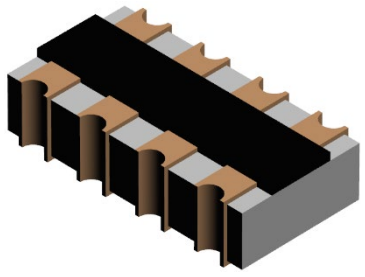
- **Pad Extension (Toe Out):** PCB land copper must extend beyond the physical side walls of the device housing. This ensures molten solder paste wicks upward into the semicircular channel, generating a visible heel fillet.
- **Solder Mask Openings:** Footprints require Non-Solder Mask Defined (NSMD) clearances around the side terminals to prevent masking material from encroaching into the castellated pocket, which could cause cold-joint connectivity failure.
- **Clearance Routing:** By keeping the outer corners of the rectangular component body free of metallic terminals, designers can safely route signal traces or drop ground via anchors right up against the corners of the housing envelope without risk of short-circuiting.

**Performance Advantages**

- **Robust Optical Inspection (AOI):** Automated optical cameras can easily view the solder fillet ascending the vertical side channel from a top-down or slight-angle camera perspective, an option missing from under-body LGA packages.
- **Self-Centering Properties:** During the reflow oven process, liquid surface tension pulling on all four concave pockets naturally realigns the chip center directly onto the target pads, reducing rotational skewing or floating.
- **Low Parasitic Loop Inductance:** Shorter internal lead pathways significantly minimize high-frequency parasitics, allowing protection diodes to react to high-speed transients rapidly

## 24.20 – Side Concave Chip Array

**Side Concave Chip Array:** A surface mount passive component housing that integrates a matrix of multiple discrete components – such as resistors or capacitors – into a single leadless chip. Rather than using protruding pins or flat bottom pads, it features multiple semi-cylindrical metallized grooves (castellations) recessed into its side walls. This format effectively places multiple independent components side-by-side in a single structural body to maximize assembly density and efficiency.



**Key Physical Features**

- **Serrated Side Castellations:** The left and right perimeter edges look like scallops or waves. The electrical terminations run up these vertical indentations, creating separate isolated contact pathways.
- **Monolithic Rectangular Body:** Constructed from a single piece of high-grade ceramic (co-fired alumina) or glass-epoxy material. This body isolates the internal passive elements from one another.
- **Even Pin Distributions:** Most commonly deployed in 4-pin (2-element), 8-pin (4-element), or 16-pin (8-element) configurations, with the contacts split symmetrically on opposite long sides.

**Footprint & Naming Parameters**

These packages follow a precise naming structure to describe their physical boundaries, using the format *RESCAV + Pin Count + P + Pitch _ Length x Width x Height + L Lead Width x Lead Length*.

Example: RESCAV8P127_500X200X70L40X80

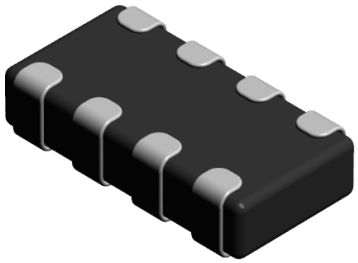
- **Pitch-Driven Layout:** The spacing between the centers of adjacent side concave pads is tightly controlled, typically standardizing at 0.50 mm or 0.80 mm.
- **Toe Pad Extension:** PCB landing pads must extend outward beyond the physical perimeter of the ceramic body to ensure the solder forms a strong, rising vertical joint.
- **Solder Mask Dams:** Pocket clearances must have precise mask dams between the closely packed side-by-side pads to prevent solder bridging during reflow.

**Performance & Manufacturing Advantages**

- **High Packing Density:** Combines up to eight individual resistors or capacitors into a single physical component footprint, saving significant board space over discrete layout methods.
- **Excellent Solder Fillet Visibility:** Solder naturally wicks up the side-wall concavities. This creates clear, visible fillets that are easily verified by Automated Optical Inspection (AOI) systems.
- **Anti-Tombstoning:** Small individual 0201 or 0402 discrete passives frequently stand up on one end during reflow (tombstoning) due to unbalanced solder forces. The larger, heavier monolithic body of a chip array completely eliminates this assembly defect.
- **Trace Routing Paths:** Because the terminations are confined strictly to the sides, the space underneath the array and around its outer corners remains completely clear, providing valuable routing room for underlying circuit traces.

## 24.21 – Side Flat Chip Array

**Side Flat Chip Array:** A surface mount passive component housing that integrates a matrix of multiple discrete components – such as resistors or capacitors – into a single leadless chip utilizing flat perimeter terminations. Unlike side *concave* chip arrays which use semi-cylindrical scalloped indentations (castellations), a side flat array features flat, continuous rectangular metal bands wrapped symmetrically around the sides of its body. This design creates a smooth, straight-edged perimeter optimized for precise component placement, highly predictable solder joint geometry, and dense layout clustering.



**Key Physical Features**

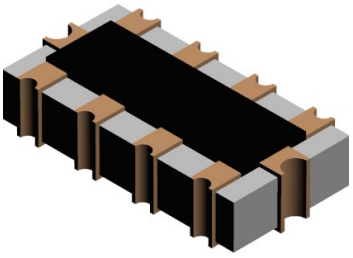
- **Flat Peripheral Terminations:** The electrical contacts consist of smooth, flat metallized bands that do not feature any scallops, curves, or indentations. They sit completely flush against the smooth outer vertical edges of the array housing.
- **Monolithic Ceramic Body:** Fabricated using a singular co-fired ceramic block (such as alumina), which isolates the internal resistive elements or capacitive layers from one another.
- **Symmetrical Layout Pinouts:** Commonly deployed in 4-pin (2-isolated elements) or 8-pin (4-isolated elements) arrays, splitting the terminations evenly along the two opposing long sides of the chip.

**Footprint & Naming Parameters**
According to the IPC-7351 standard land patterns, flat chip arrays follow a dedicated naming convention:

- **Standard Code:** Flat component arrays utilize the CAPAF (Capacitor Array, Flat) or RESAF (Resistor Array, Flat) prefixes followed by pitch and mechanical dimensions (*RESRAF + Pin Count + P Pitch + Length x Width x Height + L Lead Width x Lead Length*).
- **Predictable Toe Fillets:** Because the pads are flat and uniform, calculating the mathematical footprint model requires less toe protrusion (Jt) relative to concave packages, yielding minor space savings along the outer perimeter.
- **Narrow Solder Mask Dams:** Precise placement of solder mask web dams between the closely packed adjacent flat pads is crucial to block any solder bridging between the individual resistor/capacitor networks during high-temperature reflow.

## 24.22 – Side Concave Chip Array 4-Sided

**Side Concave Chip Array 4-Sided:** A high-density, leadless surface mount component housing that integrates a matrix of multiple passive components into a single square or rectangular chip with terminations on all four sides. Unlike standard 2-sided chip arrays, this configuration features semi-cylindrical metallized grooves (castellations) recessed into every perimeter wall. It is widely used for dense multi-resistor terminations, multi-channel capacitor arrays, and integrated EMI filtering networks.



**Key Physical Features**

- **4-Sided Concave Castellations:** Semicircular metallized scallops run up the vertical faces of all four sides. These cutouts act as individual, electrically isolated termination channels.
- **Monolithic Square Body:** The core is typically constructed from a singular co-fired ceramic (alumina) substrate that houses and isolates the internal passive elements.
- **High Pin Count Matrices:** Commonly deployed in 16-pin (8-element) or 20-pin (10-element) configurations, allowing complex parallel network routing within a single component body.

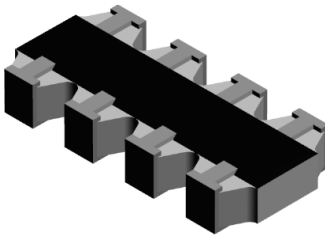
**Footprint & Naming Parameters**
These packages follow a specific naming structure to define their quad-sided boundaries:
*RESCAV + Pin Count + P Pitch _ Length x Width x Height + L Lead Width x Lead Length*
Example: RESCAV10P80_400X210X65L40X40

- **Fine Pitch Spacing:** The distance between the centers of adjacent concave channels is highly compressed, commonly standardizing at 0.50 mm or 0.65 mm.
- **Omnidirectional Toe Extension:** The PCB land copper must extend outward beyond all four edges of the physical ceramic body. This ensures molten solder paste wicks uniformly upward into every side channel.
- **Crucial Solder Mask Dams:** Because pads are closely clustered on all four sides, precise solder mask webs are required between adjacent pads to prevent cross-channel solder bridging during reflow.

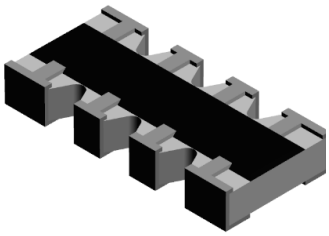
## 24.23 – Convex Chip Array

**Convex Chip Array:** A surface mount passive component housing that integrates a matrix of multiple discrete components (most commonly resistors) into a single leadless chip utilizing outward-protruding (convex) terminal pads. Unlike side *concave* chip arrays that feature semi-cylindrical recessed scallops, a convex array features smooth, bumps or lobes that extend outward beyond the main ceramic body line. It is the most ubiquitous, standard design format for high-volume resistor networks, digital bus pull-ups, and parallel damping terminations.

**Convex Chip Array Type E**



**Convex Chip Array Type S**



**Key Physical Features**

- **Outward-Bending (Convex) Leads:** The individual terminations are 5-sided blocks that bulge slightly outward from the chip side walls, optimizing contact area.
- **Larger Corner Terminations:** For most industry-standard convex packages, the four outermost corner pads are manufactured physically wider than the inner terminal pairs to anchor the component securely.
- **Monolithic Ceramic Structure:** Built on a shared high-purity alumina ceramic base substrate. Multiple independent resistive element paths are laser-trimmed and covered under a protective epoxy overcoat glass layer.
- **Pin Formats:** Symmetrically split along opposite long sides, most frequently deployed in 4-pin (2-element), 8-pin (4-element), or 16-pin (8-element) packages.

**Footprint & Naming Parameters**

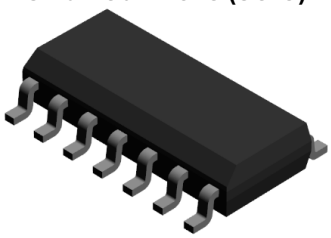
Footprint parameters, convex packages follow a strict naming structure to properly generate standard library footprints:

- **Standard Prefixes:** Uses **CRAC** (Capacitor Array, Convex) or **RESC** (Resistor Array, Convex) followed by pitch and dimensions:
  ***RESCAX*** + Pin Count + P Pitch _ Length x Width x Height + L Lead Width x Lead Length.
  Example: RESCAXS10P64_330X210X70L45X35
- **Asymmetrical Solder Pads:** Because the component corner pins are wider than the inner pins, the CAD land pattern must feature custom, wider corner pads relative to the inner pairs. Switching a PCB layout from a concave part to a convex part always mandates a solder pad re-spin.
- **Standard Spacing (Pitch):** Typically engineered on a precise 0.50 mm or 0.80 mm center-to-center lead pitch to align perfectly with automated SMT placement grids.

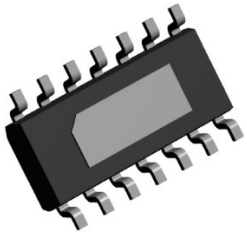
## 24.24 – Small Outline Package (SOP/SOIC)

**Small Outline Package (SOIC/SOP):** A rectangular plastic body with Gullwing leads extending outward from its two longer sides. It originally replaced bulky through-hole DIP (Dual In-line Package) components by shrinking the footprint area and vertical height by up to 70%.

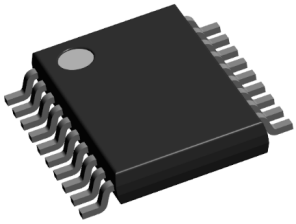
**Small Outline IC (SOIC)**



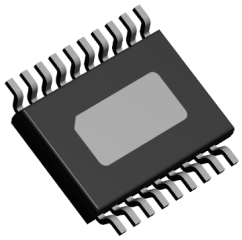
**SOIC with Thermal Tab**



**Small Outline Package (SOP)**



**SOP with Thermal Tab**



**SOP JEDEC**: MO-117, MO-118, MO-142, MO-152, MO-153, MO-180, MO-182, MO-230, MO-249, MO-271

**SOIC JEDEC:** MO-046, MO-059, MO-099, MO-119, MO-120, MO-132, MO-135, MO-137, MO-150, MO-154, MO-164, MO-174, MS-012, MS-013, MS-024, MS-025

**Key Physical Features**

- **Gullwing Leads:** Metal pins extend out from the long edges of the package and bend downward and outward, forming a shape like a gull's wing.
- **Dual-Sided Pinout:** Terminations are arranged symmetrically on opposite sides of the component body, typically numbering from 8 pins up to 64 pins.
- **Plastic Encapsulated Body:** Standard configurations utilize a rugged, flame-retardant molded epoxy resin to insulate the internal silicon die.
- **Pin 1 Identification:** A chamfered (beveled) edge on the body, a deep notch at one end, or a laser-etched dot indicates Pin 1 location.

**Body Width Variations:** SOIC packages are categorized primarily by their body width (measured across the plastic body, excluding the leads). Using the wrong width in your footprint design will prevent the component legs from touching the copper pads:

- **Narrow Body (3.90 mm):** Commonly used for lower pin counts, such as 8-pin, 14-pin, and 16-pin devices (e.g., standard logic gates, op-amps).
- **Wide Body (7.50 mm):** Typically used for higher pin counts or high-voltage chips, such as 20-pin, 24-pin, and 28-pin devices (e.g., microcontrollers, transceiver chips).

**Footprint & Design Parameters**

Standard small outline footprints follow the naming format:
SOIC or SOP + Pin Count + P Pitch _ Body Length x Lead-Span x Height + L Lead Width x Lead Length
(where Lead-Span is the tip-to-tip distance across the extended legs).
Example: SOP24P50_650X640X120L60X22

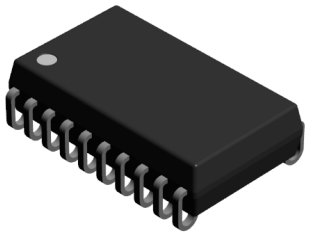
- **SOIC Standard Pin Pitch:** The center-to-center distance between adjacent pins is universally standardized at 1.27 mm. This was the original SO package in the 1980s.
- **SOP Standard Pin Pitch:** The center-to-center distance between adjacent pins is universally standardized at 0.80 mm, 0.65 mm, 0.50 mm and 0.40 mm
- **Pad Extension (Toe, Heel, and Side):** PCB landing pads must extend beyond the physical footprint of the Gullwing tip to allow a prominent solder meniscus to climb the outer face of the lead.
- **Thermal Pad Variant (SOIC-EP):** High-power variations include an Exposed Pad (EP) on the underside. This bottom pad requires a large ground-plane copper pad on the PCB filled with thermal vias to conduct heat away.

**Performance & Manufacturing Advantages**

- **High Reflow Reliability:** The mechanical flexibility of Gullwing leads acts as a suspension system, absorbing board flexing and CTE (thermal expansion) stresses without fracturing the solder joints.
- **Straightforward Inspection & Repair:** Because the pins protrude completely outside the component body, solder joints are 100% visible to standard Automated Optical Inspection (AOI) and can be easily hand-soldered or reworked with a standard soldering iron.
- **Excellent Automated Handling:** The flat top surface and rigid, widely spaced pins make it ideal for vacuum pick-and-place nozzles, ensuring fast assembly speeds and low rejection rates.

## 24.25 – Small Outline J-Lead (SOJ)

**Small Outline J-Lead (SOJ):** A rectangular, plastic-molded surface mount integrated circuit (IC) package characterized by two parallel rows of pins that curve inward underneath the chip body into a distinctive "J" shape. This design allows the component to occupy roughly 30% to 50% less board space than traditional Dual In-line Packages (DIP). It provides an incredibly robust, mechanically resilient option for high-density electronic designs. Historically, the package found its primary utilization housing high-speed memory devices.



**JEDEC**: MO-063, MO-065, MO-077, MO-088, MO-091, O-105, MO-121, MO-123, MO-124, MO-147, MO-165, MO-181, MS-023, MS-027

**Key Mechanical & Technical Specifications**

- **Lead Pitch:** Typically standardized at 1.27 mm between pin centers.
- **Body Widths:** Most common JEDEC-compliant standards specify 7.50 mm and 10.20 mm body widths.
- **Pin Counts:** Ranges broadly depending on memory architecture, typically spanning 16 to 40 pins.
- **Lead Arrangement:** Terminals protrude exclusively from the two longer parallel edges of the component.

**Core Structural Advantages**

- **Mechanical Durability & Handling:** Unlike Gullwing packages (such as the standard SOIC), the inward-folded J-leads offer exceptional bending resilience. The component can withstand aggressive automated handling, feeding tubes, and drop impacts without the leads deforming.
- **Optimized Space Efficiency:** Because the leads tuck directly beneath the plastic body rather than extending outward, the total PCB land pattern area is minimized. This layout frees up critical space on dense printed circuit boards.

**Thermal Stress Absorption:** The structural curvature of a J-lead acts as a microscopic spring. During severe thermal cycling, the leads flex to absorb differential thermal expansion stresses between the plastic package and the epoxy PCB substrate, protecting solder joints from cracking.

**Architectural Variations:** While the standard SOJ outlines remain fixed, minor application variations exist across the semiconductor landscape:

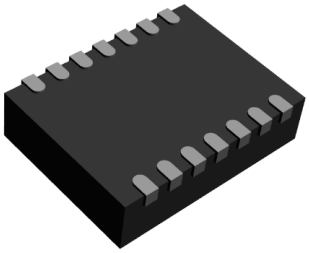
- **SOIJ (Small Outline Insulated J-Lead):** Often used interchangeably with SOJ, occasionally referencing specific Japanese EIAJ dimension configurations.
- **High-Density Modules:** Custom SOJ variants like the 42-lead package were actively registered by JEDEC to accommodate expanding memory address buses.

**Modern Industry Context:** While highly successful through the late 1980s and 1990s, the SOJ package is rarely selected for modern, cutting-edge system designs today. High-density electronics have largely transitioned to Ball Grid Array (BGA) and ultra-thin, fine-pitch packages satisfy the demand for hundreds of interconnected pins in ultra-slim form factors. However, SOJ components remain vital in legacy aerospace systems, industrial automation replacements, and retro-computing hardware upkeep.

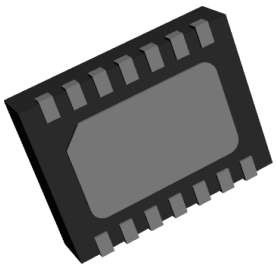
## 24.26 – Small Outline No-lead (SON)

**Small Outline No-lead (SON):** A highly compact, low-profile plastic surface mount integrated circuit (IC) package characterized by the absence of traditional protruding Gullwing or J-shaped leads. Instead, electrical contacts are established via metallized terminal pads located on the underside perimeter, completely flush with the bottom surface of the component body. Because contacts are arranged exclusively along two opposite parallel edges, it differentiates itself from the four-sided Quad Flat No-lead (QFN) format. It is also widely designated across the semiconductor industry as a Dual Flat No-lead (DFN) package by some component manufacturers.

**Small Outline No-lead (SON)**



**SON with Thermal Tab**



**JEDEC**:
MO-196, MO-197, MO-229, MO-232, MO-240, MO-245

**Key Mechanical & Technical Specifications**

- **Fine Lead Pitch:** Typically standardized at narrow spacings ranging from 0.40 mm to 0.50 mm, though variants expand up to 0.90 mm.
- **Ultra-Thin Profile:** Standard seated heights average around 0.85 mm, with ultra-thin configurations shrinking down to a mere 0.35 mm.
- **Pin Density:** Commonly deployed for smaller pin-count components, scaling tightly from 4 to 72 pins in specialized rows.
- **Thermal Enhancements:** Usually incorporates a large central Exposed Pad (EP) on the package base to function as a primary heat sink.

**Performance & Structural Advantages**

- **Superior Thermal Dissipation:** The central exposed copper die-pad is soldered directly onto the PCB's thermal land. This eliminates the thermal barrier of encapsulated plastic, letting heat flow seamlessly through plated thermal vias into internal PCB ground planes.
- **High-Frequency Electrical Signal Integrity:** Eliminating long, external lead wires massively lowers parasitic inductance, resistance, and capacitance. Consequently, SON components demonstrate clean signal performance, making them ideal for high-speed RF, wireless, and power conversion applications.
- **Drastic Space Savings:** By pulling the terminal contacts entirely under the body, the required PCB land pattern footprint shrinks significantly compared to standard SOICs. This yields high-density component clustering on complex boards.

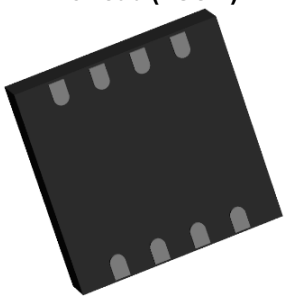
**Critical PCB Footprint & Design Guidelines:** Designing a footprint for fine-pitch SON packages demands strict attention to assembly tolerances:

- **Solder Joint Filleting:** Extend the copper land pads 0.40 mm to 0.50 mm beyond the package body perimeter (toe length). This provides proper solder paste wetting and allows for automatic optical inspection (AOI) verification.
- **Bridging Prevention:** For standard 0.50 mm pitch devices, restrict the PCB pad width to 0.28 mm or narrower. This guarantees that a solder mask web can fit safely between individual pads, preventing manufacturing shorts.
- **Thermal Pad Segmentation:** Avoid pasting a giant solid block of solder over the center exposed pad. Split the stencil aperture into a segmented grid pattern (covering 40% to 80% total area). This lets volatile flux gases escape during reflow, preventing the component from lifting or creating excessive voiding.

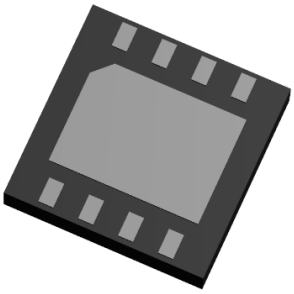
## 24.27 – Pull-back Small Outline No-lead (PSON)

**Pull-back Small Outline No-lead (PSON):** A highly specialized variant of the standard Small Outline No-lead (SON) footprint where the metallized terminal pads are deliberately recessed (pulled back) away from the outer edges of the plastic mold body. Because the electrical contacts do not reach the side walls of the IC, the molded plastic encapsulation completely encloses the outer perimeter. This structural design maximizes board routing space, reduces the risk of accidental electrical shorting, and eliminates visible external solder fillets. Component manufacturers frequently label this package family as PSON or Plastic Small Outline No-lead.

**Pull-back Small Outline No-lead (PSON)**



**PSON with Thermal Tab**



**JEDEC**: MO-209, MO-252

**The "Pull-back" Mechanism Explained:** In a standard SON or DFN/QFN package, the copper lead-frame terminal pads are cut during the singulation process, leaving exposed raw copper edges on the sides of the chip. In contrast, a PSON package pulls the terminal ends inward.

**Key Mechanical & Technical Specifications**

- **Recess Distance (Pull-back):** Terminal pads are typically shifted inward by 0.075 mm to 0.15 mm from the nominal package outline.
- **Lead Pitch:** Maintained at standard fine-pitch intervals of 0.50 mm or 0.65 mm.
- **Low Profile:** Height dimensions mirror thin variants, frequently standardizing around 0.75 mm to 0.85 mm.
- **Thermal Interface:** Incorporates a large central exposed die pad to ensure low thermal resistance.

**Architectural Benefits & Engineering Trade-offs**

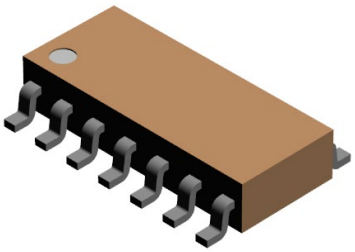
- **Creepage and Clearance Advantages:** By burying the conductive terminal pads underneath the insulating plastic body, PSON packages drastically improve creepage and clearance distances between adjacent traces on high-density layouts. This makes them popular for compact power management ICs (PMICs) and low-voltage switching regulators.
- **Reduced Perimeter Footprint:** Because the pads do not extend to the edge, PCB designers can bring peripheral components, ground fills, or trace routing closer to the IC boundary without violating safety clearances.
- **Inspection Challenges (The Solder Fillet Trade-off):** During surface mount technology (SMT) reflow, the hidden pads prevent the formation of an external side solder fillet. Because there is no visible side wetting, Automatic Optical Inspection (AOI) systems cannot verify the joint integrity by looking at the perimeter. Electronics manufacturers must rely on Automated X-Ray Inspection (AXI) to guarantee that the hidden pads are properly wetted.

**PCB Design & Stencil Requirements:** Creating a reliable footprint configuration for a PSON package requires specific modifications to your IPC-compliant CAD library:

- **Pad Inward Extension:** Unlike standard SON packages where pads extend outward to form a toe fillet, PSON footprints require the copper pads to expand slightly *inward* toward the center thermal pad to guarantee sufficient contact area.
- **Solder Mask Webbing:** Due to the pulled-back contacts, maintain a strict solder-mask-defined (SMD) or non-solder-mask-defined (NSMD) trace boundary based on the manufacturer datasheet to prevent molten paste from migrating out from under the chip.
- **Aperture Design:** Stencils should use a reduced thickness (typically 0.125 mm) with trapezoidal laser-cut walls to maximize paste release on the small, recessed land patterns.

## 24.28 – Ceramic Flat Package (CFP)

**Ceramic Flat Package (CFP):** A highly specialized, hermetically sealed surface mount integrated circuit (IC) package utilized almost exclusively in military, aerospace, and high-reliability deep-space electronics. It features a ceramic base and lid bonded together with parallel rows of thin metal ribbons or Gullwing leads extending from its sides. Unlike commercial plastic packages, the CFP provides total immunity to moisture ingress, chemical corrosion, and intense radiation fields, making it the industry benchmark for operating in extreme, unforgiving environments.



**JEDEC**: MO-018, MO-020, MO-021, MO-022, MO-023, MO-032, MO-070, MO-092, MO-098, MO-106, MO-115, MO-146, MS-033

**Key Mechanical & Technical Specifications**

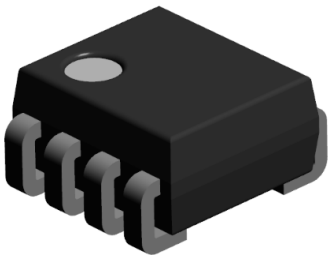
- **Hermetic Construction:** Utilizes high-purity aluminum oxide ceramic bodies co-fired with tungsten or gold-plated Kovar metal configurations.
- **Lead Pitches:** Typically features standard fine-pitch spacings of 1.27 mm or 0.635 mm.
- **Pin Counts:** Highly customizable, ranging from small 14-pin logic gates up to high-density 84-pin or 100+ pin complex microprocessors.
- **Lead Forms:** Components are often shipped with flat, unformed metal ribbon leads, allowing assembly houses to custom-bend them into Gullwing configurations prior to soldering.

**Architectural Performance Advantages**

- **Ultimate Hermeticity & Environmental Immunity:** Plastic encapsulated chips eventually absorb ambient moisture, which can cause internal corrosion or "popcorning" during thermal shock. CFP packages use a glass or gold-tin eutectic weld to fuse the ceramic lid to the base. This provides a true hermetic seal that completely blocks moisture, gases, and atmospheric contaminants.
- **Low Thermal Expansion Matching:** The coefficient of thermal expansion (CTE) of aluminum oxide ceramic is much lower than standard FR-4 epoxy board substrates but matches perfectly with specialized polyimide or metal-core PCBs used in aerospace. This parity prevents structural mechanical warping and trace shear stress when components experience sudden, massive temperature swings.
- **Exceptional Outgassing Resistance:** In a vacuum environment like space, volatile organic compounds within standard plastic components evaporate (outgas) and condense onto sensitive optical lenses, solar arrays, or high-voltage circuits. Because ceramic and glass are inorganic, CFP packages exhibit virtually zero outgassing, ensuring payload safety.

## 24.29 – Small Outline L-Lead (SOL)

**Small Outline L-Lead (SOL):** A variation of the surface mount integrated circuit package where the parallel rows of pins exit the side of the plastic mold compound, bend downward, and then curve inward underneath the IC body. While a traditional "L-lead" or Gullwing package flares outward to maximize solder joint visibility, the inward L-lead folds back under the component body. This structural geometry functions very similarly to a J-lead package (SOJ), but utilizes flat, right-angle ribbon leads instead of rounded, J-shaped wires. This specialized configuration delivers a low-profile, mechanically stable connection tailored for strict high-density board layouts.



**Key Mechanical & Technical Specifications**

- **Lead Profile:** Features flat ribbon leads bent at a sharp 90-degree angle that point directly toward the center axis of the chip.
- **Lead Pitch:** Typically spaced at standard intervals of 1.27 mm or fine-pitch variations of 0.65 mm, depending on the vendor's package registry.
- **Footprint Efficiency:** Reduces total board area consumption by roughly 20% to 35% compared to an outward-facing Gullwing SOIC layout.
- **Component Height:** Maintains a low seated profile, typically between 1.50 mm and 2.50 mm.

**Engineering Advantages**

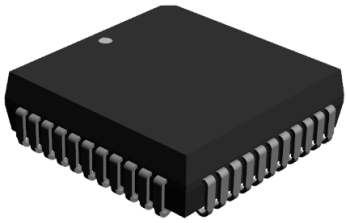
- **Enhanced Lead Alignment & Coplanarity:** Because the leads fold tightly against the underside of the component body, they are significantly less prone to accidental deformation or bending during shipping, automated tape-and-reel feeding, and high-speed pick-and-place handling. This rigidity preserves strict coplanarity across all pins prior to reflow.
- **Structural Stress Mitigation:** The flat, right-angled section tucked beneath the chip provides uniform surface contact with the PCB pads. This distributes mechanical shock and differential thermal expansion loads evenly across the joint, lowering the likelihood of trace shear failure or brittle fracturing.
- **High Concentration Board Clusters:** Eliminating outward-flaring Gullwings allows PCB designers to route traces, place vias, or locate decoupling capacitors immediately adjacent to the plastic body walls without risking electrical shorts.

**SMT Manufacturing & Layout Considerations:**
Implementing an inward SOL component requires unique adjustments to your stencil printing and quality control workflows:

- **Footprint Land Pattern:** The copper target pads must shift completely beneath the nominal component outline. A tiny toe extension (around 0.15 mm to 0.25 mm) should be maintained past the bend shoulder to establish a minimal visible solder boundary.
- **Aperture & Paste Control:** Because the leads sit directly under the plastic shell, precise solder paste volume is necessary. Excess paste cannot migrate outward safely and may result in solder balling or bridging under the package body.
- **Inspection Constraints:** The inward bend heel fillet is from top-down optical line-of-sight. While basic Automated Optical Inspection (AOI) can check for gross skewing or toe wetting under the package, high-reliability assemblies use Automated X-Ray Inspection (AXI) to fully verify the structural voiding and bond quality underneath the body.

## 24.30 – Plastic Leaded Chip Carrier (PLCC)

**Plastic Leaded Chip Carrier (PLCC):** A Square or rectangular surface mount integrated circuit (IC) package featuring J-shaped leads arranged along all four perimeter edges. Like the two-sided SOJ package, its pins exit the side of the plastic mold compound and curve inward underneath the component body. PLCCs can be soldered directly onto a PCB land pattern or plugged into specialized through-hole or surface mount PLCC sockets. This multi-functional integration made them an industry standard for housing erasable and programmable devices like microcontrollers, flash memory, and BIOS chips throughout the 1990s and 2000s.



**JEDEC**: MO-044, MO-047, MO-087, MO-107, MO-110, MS-006, MS-007, MS-016, MS-018

**Key Mechanical & Technical Specifications**

- **Lead Pitch:** Standardized globally at a wide, highly manufacturable 1.27 mm spacing.
- **Form Factors:** Available in Square shapes (equal pin count on all four sides) and Rectangular shapes (asymmetric pin distribution).
- **Pin Counts:** Typically scales across standard JEDEC sizes, spanning 20, 28, 44, 52, 68, and 84 pins.
- **Package Height:** Thick relative to modern packages, typically ranging from 3.18 mm to 4.57 mm.

**Architectural Advantages & Socket Utility**

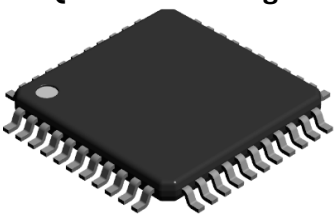
- **In-System Swappability via Sockets:** The defining advantage of the PLCC is its compatibility with sockets. When soldered to a socket, a PLCC chip can be extracted using a specialized tool and replaced without desoldering. This provides a low-cost method for updating firmware, modifying BIOS code, or swapping out damaged controllers in the field.
- **Robust Lead Protection:** Because the J-shaped pins curl directly underneath the heavy plastic body, the pins are completely shielded from accidental bending during bulk shipping, manual handling, or insertion into high-friction test sockets.
- **Excellent Thermal and Flex Compliance:** The structural curvature of the four-sided J-leads functions as an omnidirectional spring. When a PCB undergoes thermal expansion or mechanical flexing, the leads flex along both axes to absorb the stress, protecting the underlying solder joints from cracking.

**Modern Industry Application:** While largely phased out of ultra-compact commercial electronics in favor of QFP, QFN, and BGA packages, PLCCs and their corresponding sockets remain heavily utilized in industrial automation controllers, telecommunications infrastructure, legacy computing hardware maintenance, and automotive diagnostic equipment.

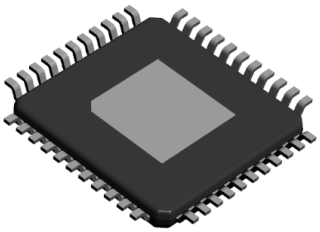
# 24.31 – Quad Flat Package (QFP)

**Quad Flat Package (QFP):** A square or rectangular surface mount integrated circuit (IC) package featuring Gullwing (L-shaped) leads extending outward from all four perimeter edges. This design allows it to accommodate much higher pin counts than two-sided packages like SOIC or SOJ. The QFP serves as a critical bridge between low-pin-count small outline packages and complex ball grid arrays. It became the global industry standard for housing microcontrollers, digital signal processors (DSPs), and application-specific integrated circuits (ASICs) throughout consumer electronics, automotive modules, and industrial hardware.

**Quad Flat Package**



**Quad Flat Package with Thermal Tab**



**JEDEC**: MO-071, MO-082, MO-084A, MO-108, MO-112, MO-173, MO-198, MO-212, MS-022, MS-029
**JEDEC** (with thermal): MO-114, MO-189, MO-204, MS-026

### Key Mechanical & Technical Specifications

- **Lead Pitch:** Typically ranges from fine to ultra-fine pitches, spanning 0.40 mm, 0.50 mm, 0.65 mm, 0.80 mm.
- **Pin Counts:** Highly scalable, commonly ranging from 32 pins up to 200+ pins.
- **Component manufacturer Body Profiles:** Package thicknesses vary widely across component manufacturers. However, the standard footprint name prefix for all these variations is QFP.
    - **LQFP (Low-Profile QFP):** Standardized at a fixed body thickness of 1.60 mm.
    - **TQFP (Thin QFP):** Slimmed down to a maximum body thickness of 1.20 mm.
    - **VTQFP (Very Thin QFP):** Maximum body thickness of 0.80 mm.
    - **PQFP (Plastic QFP):** Older, thicker variants ranging from 2.00 mm to 3.40 mm, often featuring protective bumper corners.

### Core Engineering & Assembly Advantages

- **Exceptional Solder Joint Inspectability:** Because the Gullwing leads flare outward away from the plastic package body, every single solder connection is completely visible from above. This allows high-speed Automatic Optical Inspection (AOI) systems or manual inspectors to verify heel and toe wetting fillets easily without requiring expensive X-ray imaging.
- **High Interconnect Density:** Distributing interconnect pins along all four edges significantly decreases the required PCB surface area compared to dual-side leaded packages. This allows dense, multi-channel microcontrollers to fit onto compact circuit boards.
- **Compliance and Stress Absorption:** The mechanical "S" or "L" bend in each Gullwing lead acts as a microscopic spring. When the underlying PCB expands, contracts, or flexes due to thermal changes and mechanical vibrations, the leads absorb the stress to prevent the solder joints from cracking.

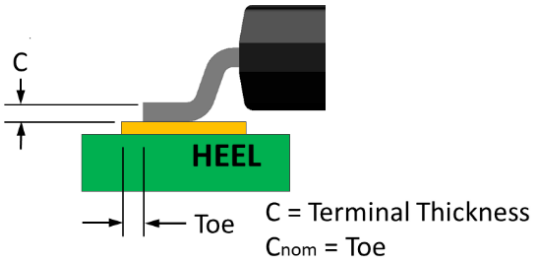
### Structural Variations

To meet expanding power and thickness constraints, the QFP design has evolved into several specialized configurations:

- **HQFP (Heat-sink QFP):** Integrates a metal heat spreader or an exposed copper pad on the top or bottom surface to dissipate thermal energy from high-power chips.
- **CQFP (Ceramic QFP):** Replaces the plastic compound with a hermetically sealed ceramic body for extreme aerospace, defense, and high-reliability deep-space environments.

**PCB Land Pattern & Design Constraints:** Designing a reliable land pattern for fine-pitch QFPs requires tight layout tolerances to prevent manufacturing defects:

- **Solder Bridging Prevention:** For fine pitches (0.40 – 0.50 mm), the copper pads must be narrow (typically 0.22 mm to 0.28 mm wide). This leaves a safe gap for a solder mask dam (web) between adjacent pads to prevent molten paste from bridging during reflow.
- **Toe and Heel Fillets:** The PCB Toe Fillet should be 100% the nominal height of the terminal lead and the Pad Heel should be the distance from the Terminal Heel to the nominal package body to give the solder paste room to form proper structural fillets.

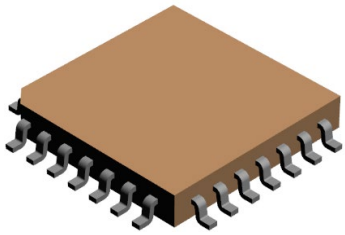



| FED Gull Wing Terminal Solder Joint Goal for Determining the Toe Value | | |
|---|---|---|
| Terminal Lead Pitch | Cnom | Toe |
| >= 1.00 mm | 0.35 | 0.35 |
| >= 0.80 and < 1.00 mm | 0.30 | 0.30 |
| >= 0.65 and < 0.80 mm | 0.25 | 0.25 |
| >= 0.50 and < 0.65 mm | 0.20 | 0.20 |
| >= 0.40 and < 0.50 mm | 0.15 | 0.15 |
| <= 0.40 mm | 0.15 | 0.15 |

Coplanarity Sensitivity: Because QFP leads are thin and extend outward, they are easily bent during shipping or manual handling. If a single lead is lifted out of alignment by more than 0.08 mm to 0.10 mm, it will fail to touch the solder paste pad, resulting in an open circuit.

## 24.32 – Ceramic Quad Flat Package (CQFP)

**Ceramic Quad Flat Package (CQFP):** A Premium, hermetically sealed surface mount integrated circuit (IC) package designed specifically for aerospace, defense, deep-space, and high-reliability industrial applications. It features flat ribbon or Gullwing leads extending from all four perimeter edges of a high-purity ceramic body. By combining the four-sided, high-pin-count architectural layout of a standard Plastic Quad Flat Package (QFP) with the absolute environmental immunity of co-fired ceramic materials, the CQFP functions as the industry-standard housing for space-grade FPGAs, high-speed microprocessors, and complex digital signal processors (DSPs).



**JEDEC**: MO-081, MO-090, MO-104, MO-111, MO-125

**Key Mechanical & Technical Specifications**

- **Hermetic Material:** Constructed from multilayer aluminum oxide or aluminum nitride ceramic, sealed with a gold-tin (AuSn) eutectic alloy or glass-frit weld.
- **Lead Pitch:** Typically standardized at fine-pitch spacings of 0.635 mm or 1.27 mm to handle high routing densities.
- **Pin Counts:** Highly scalable to support complex silicon architecture, commonly ranging from 68 pins up to 352+ pins.
- **Lead Delivery State:** Frequently shipped in a "flat" unformed state protected by a metal tie-bar matrix. Assembly facilities trim the tie-bar and bend the ribbon leads into customized Gullwing shapes just prior to PCB placement.

**Critical Engineering & Performance Advantages**

- **Absolute Hermeticity:** Unlike standard plastic packages that slowly absorb atmospheric moisture over time, the CQFP's ceramic-to-metal seals form an absolute gas-tight barrier. This prevents moisture ingress, eliminating internal corrosion, wire-bond degradation, and the destructive "popcorning" effect during rapid thermal transitions.
- **Radiation Hardening Support:** Space environments present intense cosmic and solar radiation fields that degrade standard commercial silicon. The dense ceramic composition and heavy gold plating of CQFP housings provide an inherent layer of physical shielding against alpha particles and electromagnetic interference (EMI).
- **Coefficient of Thermal Expansion (CTE) Matching:** The CTE of aluminum oxide ceramic closely matches advanced substrate materials like polyimide-glass, metal-core boards, or copper-invar-copper (CIC) cores. This parity minimizes structural shear stress on the solder joints when aerospace modules undergo extreme temperature cycling from 65° C in orbit to +150° C during atmospheric re-entry.
- Exceptional Thermal Dissipation: High-pin-count CQFPs frequently integrate a massive metal or ceramic base plate (exposed pad) on either the top or bottom surface. Soldering or mechanically clamping this pad to a dedicated PCB thermal plane drastically reduces junction-to-case thermal resistance.

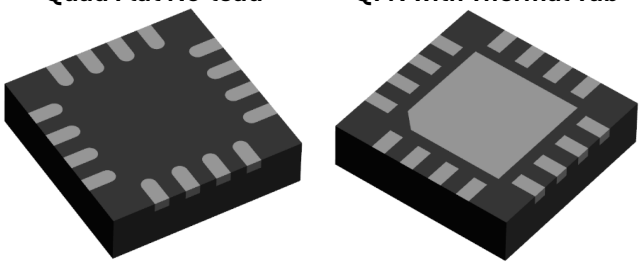
**PCB Design & Specialized Assembly Rules:** Due to the strict quality demands of aerospace standards (such as NASA-STD-8739.3 or MIL-STD-883), laying out a land pattern and assembling a CQFP requires rigorous process controls:

- **Tie-Bar Trimming & Lead Forming:** Unformed flat ribbon leads must be processed using ultra-precise, automated tool dies to create uniform Gullwing configurations. Manual bending is prohibited in high-reliability workflows, as minor variations compromise lead coplanarity and induce micro-cracks in the lead plating.
- **Toe, Heel, and Side Fillet Validation:** Footprint target pads must extend significantly past the formed lead boundaries (the toe is equal to the terminal lead thickness, and the Heel is equal to the terminal heel to the nominal package edge). This allows the solder paste to form distinct, highly visible fillets required for strict visual inspection without automated X-ray dependency.
- **Mechanical Tie-Downs and Underfills:** Because ceramic bodies are heavy, intense launch vibrations can snap thin copper traces or crack solder joints. Space-grade layouts often dictate the application of specialized silicone or epoxy underfills beneath the component body to decouple mechanical G-forces from the electrical contacts.

## 24.33 – Quad Flat No-lead (QFN)

**Quad Flat No-lead (QFN):** A highly popular, low-profile surface mount integrated circuit (IC) package characterized by a square plastic body with no protruding lead wires. Instead, it utilizes metallized terminal pads arranged along all four edges of its underside perimeter, completely flush with the bottom surface of the component. It is the four-sided counterpart to the Small Outline No-lead (SON) package and is widely favored for modern smartphones, consumer electronics, and high-frequency RF modules due to its miniature footprint and excellent electrical characteristics.

**Quad Flat No-lead** **QFN with Thermal Tab**



**JEDEC**: MO-220, MO-241, MO-243, MO-248

**Key Mechanical & Technical Specifications**

- **Fine Lead Pitch:** Standardized at tight sub-millimeter intervals, most commonly 0.40 mm, 0.50 mm, 0.65 mm and 0.80 mm.
- **Ultra-Low Profile:** Seated package heights are exceptionally slim, typically ranging from 0.75 mm down to 0.40 mm.
- **Pin Counts:** Highly scalable for small-to-medium logic circuits, ranging from 8 pins up to 100+ pins.
- **Thermal Core:** Features a prominent central Exposed Pad (EP) on the underside to facilitate direct thermal and electrical grounding.

**Core Engineering & Performance Advantages**

- **Minimal Parasitic Inductance:** By eliminating long, external Gullwing or J-shaped leads, the internal wire bonds or flip-chip bumps connect almost directly to the PCB copper. This short path drastically reduces parasitic inductance, resistance, and capacitance, allowing QFNs to operate cleanly in high-speed digital and high-frequency RF applications.
- **High-Efficiency Thermal Path:** The central exposed metal die pad is designed to be soldered directly to the board's copper plane. This configuration allows heat generated by the silicon die to bypass the plastic encapsulation completely, transferring directly into internal PCB copper layers via plated thermal vias.

**Substantial PCB Space Savings:** Because the contacts are pulled entirely underneath the perimeter of the component body, a QFN consumes up to 60% less board area and 30% less height than an equivalent leaded package like a Quad Flat Pack (QFP).

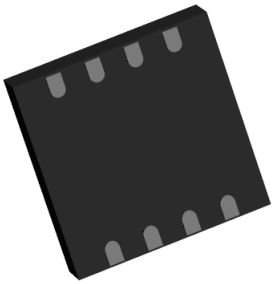
**PCB Land Pattern & Manufacturing Challenges:** Designing an IPC-7351 compliant footprint for a fine-pitch QFN package requires balancing compact spacing with assembly reliability:

- **The Solder Fillet Dilemma (Toe Fillets):** QFN lead-frames are typically cut during factory singulation, leaving raw, unplated copper exposed on the outer sides of the chip. This exposed copper oxidizes rapidly. During reflow, solder paste will wet the bottom pad perfectly but may fail to climb up the outer side wall. Because there is no reliable side fillet, Automatic Optical Inspection (AOI) systems struggle to verify joint quality, often necessitating Automated X-Ray Inspection (AXI).
- **Wettable Flanks (An Assembly Fix):** To solve the AOI issue, many modern QFNs feature a step-cut or plated cavity on the outer edge called a Wettable Flank. This manufacturing process keeps the outer edge of the pad plated with gold or tin, forcing the solder paste to form a visible vertical fillet that standard AOI cameras can easily verify.
- **Thermal Paste Segmentation:** To prevent the component from floating or tilting during reflow, the solder paste stencil aperture over the large center pad must not be a single giant opening. Designers must divide the center stencil aperture into a segmented matrix grid (covering 50% to 75% of the area) to let volatile flux gases escape without creating massive solder voids.
- **Solder Mask Dams:** For ultra-fine pitches (≤ 0.50 mm), the space between individual perimeter pads is incredibly narrow. Maintain a strict pad-to-mask clearance boundary to ensure the PCB fabricator can successfully place an insulating solder mask web between the pads, preventing solder bridging.

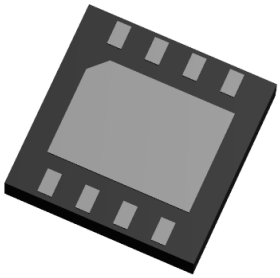
## 24.34 – Pull-back Quad Flat No-lead (PQFN)

**Pull-back Quad Flat No-lead (PQFN):** A high-power surface mount package. It features exposed metal pads underneath its perimeter rather than traditional extending pins. The "pull-back" design exposes wettable flanks on the package edges, allowing for visible solder fillets during automated optical inspection (AOI) to guarantee reliable board mounting.

**Pull-back Small Outline No-lead**



**PSON with Thermal Tab**



**JEDEC**: MO-208

**Key Package Characteristics**

- **Design & Layout:** Instead of extending leads, electrical and thermal connections are made through flat contact pads located on all four sides of the package's underside.
- **Thermal Management:** The bottom of the package features one or more exposed copper die-pads (or heat sinks). These act as direct thermal pathways to pull heat efficiently away from the silicon die and into the PCB.
- **Wettable Flanks:** The "pull-back" feature means the package body slightly recedes from the outer edges of the terminal pads. This exposes the side of the leads, allowing solder to creep up and form a visual fillet.
- **Electrical Performance:** Because there are no long, protruding leads, electrical parasitics (such as lead inductance and signal resistance) are dramatically reduced

**Advantages and Applications**

- PQFN packages are highly favored for power-dense electronic applications where space is limited but thermal loads are high. The wettable flank "pull-back" design is particularly crucial for automotive, aerospace, and high-reliability industrial applications, where board manufacturers rely on visual or X-ray inspections rather than blind electrical tests to ensure zero-defect assembly.
- For board-level assembly, specific land patterns and stencil designs are required to ensure robust solder coverage between the package pads and the circuit board.

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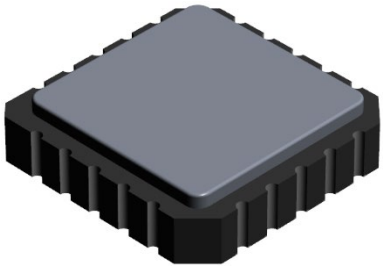
## 24.35 – Leadless Chip Carrier (LCC)

**Leadless Chip Carrier (LCC):** A rugged, surface mount integrated circuit package that uses flat metal pads instead of pins. It features a ceramic body, making it highly resistant to extreme temperatures and harsh environments.



**JEDEC**: MO-027, MO-041, MO-042, MO-075, MO-085, MS-003, MS-004, MS-005, MS-009, MS-014

**Key Package Characteristics**

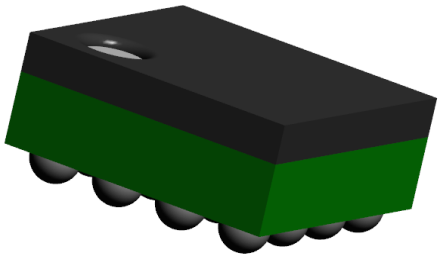
- **No Physical Leads:** Electrical connections are made via gold-plated metallic pads (castellations) tucked into the perimeter of the package.
- **Ceramic Construction:** The hermetically sealed ceramic body provides exceptional protection against moisture, heat, and shock.
- **High-Reliability Inspection:** The castellations extend up the sides of the package, creating visible solder joints for easy inspection.
- **Thermal Expansion Match:** Its thermal expansion rate closely matches specific PCB substrates like ceramic-core boards, preventing solder joints from cracking.

**Advantages and Applications**

- LCC packages are widely used in military, aerospace, and high-temperature industrial systems due to their durability and airtight seal. Because they lack long lead wires, they exhibit very low parasitic inductance and capacitance, making them ideal for high-frequency RF and microwave applications.
- However, because ceramic is rigid, soldering LCCs directly to standard FR4 fiberglass boards can lead to joint failure under thermal stress. For commercial applications where standard FR4 boards are used, designers typically switch to the Plastic Leaded Chip Carrier (PLCC), which uses flexible "J-shaped" metal leads to absorb this physical stress.

## 24.36 – Ball Grid Array, Collapsing Ball (BGA)

**Ball Grid Array, Collapsing Ball (BGA):** A high-density, surface mount integrated circuit package that uses an array of solder spheres for electrical and thermal connections. In this specific configuration, standard eutectic or near-eutectic solder balls melt completely during the reflow process, causing the package height to drop or "collapse" onto the PCB pad.



**JEDEC**: MO-149, MO-156, MO-158, MO-159, MO-192, MO-195, MO-205, MO-294, MO-298, MO-301, MO-302, MO-304, MO-307, MO-308, MO-311, MS-028, MS-034

**Key Package Characteristics**

- **Grid Array Layout:** Connections cover the entire bottom surface of the package rather than just the perimeter, maximizing pin count per unit area.
- **Controlled Collapse:** The solder balls flow entirely during assembly, relying on surface tension to align the package and self-center it over the PCB pads.
- **Standoff Control:** The final height between the package and the PCB is determined by the volume of the solder paste, pad sizes, and the weight of the component.
- Short Signal Paths: Eliminating wire leads lowers parasitic inductance and resistance, resulting in excellent high-speed electrical performance.

**Advantages and Applications**

- Collapsing BGA packages are the industry standard for high-performance processors, FPGAs, chipsets, and dense memory modules. The self-aligning nature of the collapsing balls dramatically reduces assembly defects during automated manufacturing. Additionally, the full grid layout provides ample paths for ground and power shielding, lowering electromagnetic interference (EMI).
- Because the balls collapse completely, careful engineering of the PCB pad geometry is critical. Designers must choose between Non-Solder Mask Defined (NSMD) pads for higher mechanical trace reliability, or Solder Mask Defined (SMD) pads for stricter standoff height control and resistance to thermal stress cracking.

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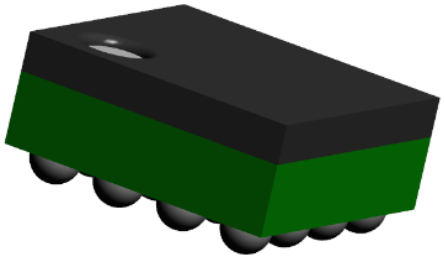
## 24.37 – Ball Grid Array, Non-collapsing Ball (BGA)

Ball Grid Array, Non-collapsing Ball (BGA): A high-density, surface mount package designed to maintain a rigid, predictable standoff height during assembly. Unlike standard BGAs, the solder spheres do not melt during the reflow process; instead, a separate, lower-melting-point solder paste connects the rigid spheres to the PCB pads.



**JEDEC**: MO-149, MO-156, MO-158, MO-159, MO-192, MO-195, MO-205, MO-294, MO-298, MO-301, MO-302, MO-304, MO-307, MO-308, MO-311, MS-028, MS-034

**Key Package Characteristics**

- **Fixed Standoff Height:** The high-melting-point spheres remain solid during reflow, ensuring a guaranteed clearance gap between the package and the PCB substrate.
- **High-Melting Materials:** The spheres typically consist of high-lead alloys (like 90Pb/10Sn) or copper-cored columns that survive standard reflow temperatures (220°C to 260°C).
- **Reliable Void Clearance:** The fixed clearance gap allows flux residues to be easily washed away and prevents the package from tilting or shorting out adjacent pads.
- **Stress Relief:** The rigid standoff absorbs differential thermal expansion between large ceramic packages and standard FR4 boards, preventing joint cracking.

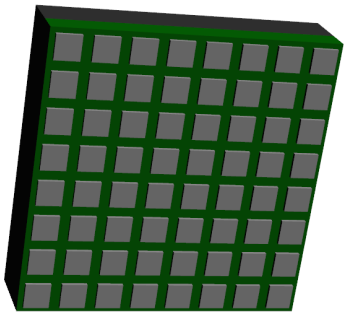
**Advantages and Applications**

- Non-collapsing BGAs are often referred to as Ceramic Ball Grid Arrays (CBGA) or plastic packages with specialized core balls – are heavily utilized in high-reliability servers, aerospace guidance systems, and telecom infrastructure. The guaranteed standoff height is highly beneficial for routing heavy RF signals, as it keeps parasitic capacitance between the chip substrate and the motherboard perfectly uniform.
- Because the structural sphere does not melt, achieving a reliable joint requires precise control over

the volume of the printed solder paste. For this reason, Solder Mask Defined (SMD) pads are frequently preferred on the PCB side to strictly control the wetting area and maximize the fatigue life of the joint under heavy thermal cycling.
- Via-in-Pad technology is normally used to fanout these fine pitch non-collapsing BGAs.

## 24.38 – Land Grid Array (LGA)

Land Grid Array (LGA): A high-density surface mount integrated circuit package that replaces protruding leads or solder balls with an array of flat, gold-plated copper pads (lands) on its underside. Unlike BGA packages, an LGA does not come with pre-attached solder spheres, making it much thinner and allowing it to be either soldered directly to a PCB or mounted into a specialized hardware socket.



**JEDEC**: MO-222

**Key Package Characteristics**

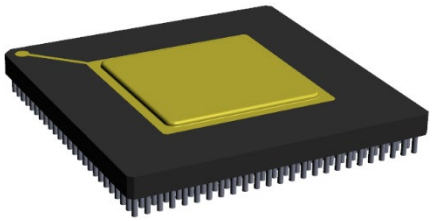
- **Flat Contacts:** The interface consists entirely of flat, coplanar metal pads arranged in a grid across the bottom surface of the component.
- **Low Profile:** Eliminating solder balls minimizes the standoff height, creating an ultra-thin package profile ideal for space-constrained designs.
- **Dual Mounting Options:** Can be permanently soldered down via surface mount technology (SMT) or placed into an LGA socket for easy replacement, upgrading, or testing.
- **Superior Signal Integrity:** The exceptionally short electrical path between the silicon die and the motherboard yields minimal parasitic inductance, maximizing high-speed data performance.
- **Robust Coplanarity:** Without delicate pins or fragile solder balls to bend or damage during handling, the package is mechanically highly robust prior to assembly.

**Advantages and Applications**

- LGA packages are the industry standard for high-performance computing hardware, such as desktop and server microprocessors (Intel, Xilinx, NVIDIA, AMD, Analog Devices CPUs), where socketing allows for modular upgrades. Because of their excellent thermal dissipation and low signal distortion, they are also widely adopted in high-frequency RF modules, network switches, 5G baseband processors, and miniature MEMS sensors.
- When soldering an LGA directly to a PCB, manufacturing requires strict control. Because the standoff height between the package and the board is minimal (often less than 0.10 mm), getting the solder paste stencil thickness correct is vital to avoid short-circuits between pads. Additionally, proper venting pathways must be designed into the PCB layout to allow volatile flux gases to escape during the reflow process, preventing voids in the solder joints.

## 24.39 – Column Grid Array (CGA)

Column Grid Array (CGA): An ultra-high-density, high-reliability surface mount package designed specifically to handle extreme thermal and mechanical stress. Instead of using solder balls or flat pads, a CGA utilizes an array of high-temperature solder columns on its underside. This unique structural architecture provides a flexible, tall standoff height that absorbs physical distortion between the component and the circuit board.



**Key Package Characteristics**

- **Column Array Interface:** Tiny, vertical cylinders (columns) are attached to the bottom of the package substrate in a grid layout.
- **High Standoff Clearance:** The extended height of the columns provides a substantial physical gap between the package body and the PCB.
- **Strain Relief Mechanics:** The tall columns act like tiny springs. They flex slightly to absorb differential thermal expansion (CTE mismatch) between rigid ceramic substrates and standard FR4 circuit boards.
- **Thermal Shock Resistance:** By flexing under stress, the columns prevent the solder joints from cracking during rapid, extreme temperature cycles.
- **Non-Collapsing Structure:** The columns are made from high-melting-point alloys that remain completely solid during standard assembly reflow.

**Advantages and Applications**

- CGA packages, frequently designated as Ceramic Column Grid Arrays (CCGA) are the gold standard for aerospace, military, defense, and deep-space satellite systems. Large, complex devices like space-grade FPGAs and high-end military processors generate significant heat and must endure severe vibrational forces. Standard BGA solder joints would quickly crack under these conditions, but CGA columns absorb the stress to ensure a long operational lifespan.
- Manufacturing with CGA components requires highly specialized process controls. Because the columns cannot collapse to self-level, the PCB planarity must be near-perfect. Additionally, due to the tight spacing and high standoff height of the columns, post-assembly cleaning processes must be carefully designed to ensure all aggressive flux residues are thoroughly washed away from underneath the large package body.

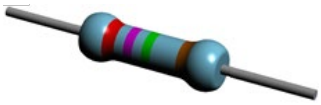
# 25.0 – Through-hole Component Families

## 25.1 – Axial Leaded Components

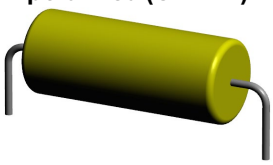
A type of through-hole electronic package featuring a symmetrical body with conductive wire leads extending from opposite ends along its longitudinal axis. This straight-line design creates a distinct "arm-like" look that sets it apart from radial components, whose leads emerge parallel from a single side like legs.

**Non-polarized Axial Lead Packages:**

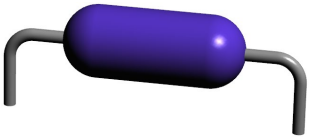
**Resistor (RESAD)**



**Capacitor Non-polarized (CAPAD)**



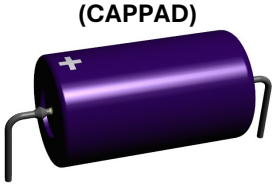
**Fuse Axial Diameter (FUSAD)**



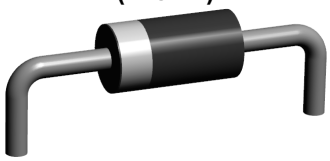
**Inductor Axial Diameter (INDAD)**

**Polarized Axial Lead Packages:**

**Capacitor Polarized Axial Diameter (CAPPAD)**



**Diode Axial Diameter (DIOAD)**



**JEDEC**: DO-007, DO-014, DO-015, DO-016, DO-026, DO-029, DO-032, DO-034, DO-035, DO-039, DO-041

**Core Geometry and Structure**

- **The Body:** The central housing is typically cylindrical or bar-shaped. It protects the internal active or passive element (such as a ceramic formula, carbon composition, or semiconductor junction).
- **The Leads:** Two solid, single-strand tinned copper wires extend outward in opposite directions along the exact center line of the body. For heavy-current applications like high-capacity fuses, these leads may occasionally feature stranded or braided wire.

**Typical Markings and Identification**

- **Resistors:** The body features concentric, brightly colored rings. These rings utilize a standardized color code to explicitly define the component's resistance, multiplier, and tolerance values.
- **Diodes:** A single, high-contrast solid stripe or band is painted near one edge. This band explicitly marks the cathode (negative terminal) to prevent incorrect orientation during assembly.
- **Capacitors:** Cylindrical axial capacitors often print specifications – such as capacitance (uF) and voltage limits – directly onto the outer sleeve. Polarity is indicated by a chamfered edge, an indented groove, or a minus sign (–) arrow pointing toward the negative terminal.

**Mechanical Installation Forms**

Axial components are highly adaptable and require manual or automated lead-forming before insertion into a printed circuit board:

- **Horizontal Mount (Standard):** The leads are bent 90° downward at equal distances from the body. The body sits flat or slightly elevated, resting snugly and parallel to the board surface between two distinct through-holes.
- **Vertical Mount (Goalpost / Panasert):** One lead is bent entirely backward 180° to run parallel alongside the component body. This effectively mimics a radial component layout, reducing the total board surface area used at the expense of vertical overhead clearance

## 25.2 – Radial Leaded Components

A through-hole electronic package where all conductive leads emerge from a single surface, typically the bottom of the component body. This architecture allows the part to stand upright on a printed circuit board (PCB), taking up significantly less surface area than an axial component.

### 25.2.1 – Dipped

A through-hole component characterized by an irregular, bulbous, organic-shaped body formed by liquid encapsulation. Instead of being housed in rigid plastic boxes or molded cylindrical cans, these capacitors are manufactured by submersing the raw internal element into a protective liquid bath. Both wire terminals emerge parallel to each other from the bottom of the component base.

**JEDEC**: MO-001, MO-015, MO-016, MO-024, MO-036, MO-037, MO-038, MO-039, MO-043, MO-095, MO-103, MO-122, MS-001, MS-010, MS-011, MS-015, MS-019, MS-020, MS-021, MS-030, MS-031, MS-032

**Outer Coating and Texture**

- **The "Dip" Finish:** The body is encapsulated in a conformal coating of epoxy resin or phenolic resin. This liquid application gives the component smoothed, teardrop, or pebble-like rounded edges that take the shape of the underlying internal dielectric layers.
- **Visual Thickness Variance:** The coating thickens significantly near the base, forming a characteristic resin droplet bead right where the copper wire leads enter the component body.
- **Colors:** They are most commonly coated in distinctive glossy or matte industrial colors, including vibrant blue, golden-yellow, dark amber, orange, or deep green

**Geometry and Common Types**

The underlying internal dielectric structure directly determines the shape of the outer dipped shell:

| Capacitor Type | Physical Shell Shape | Visual Features |
|---|---|---|
| Dipped Tantalum | Teardrop or Oval | Asymmetrical, bulbous bead with a hard, glossy finish. |
| Multilayer Ceramic (MLCC) | Squarish or Rounded Rectangle | Compact pillow-shape; small footprint. |
| Dipped Silver Mica | Flat, Broad Pillow | Distinctly wide, compressed body with sharp edge transitions. |
| Dipped Film | Puffy, Wide Slab | Chunky, elongated rectangle with smoothed, heavily rounded corners. |

**Lead and Component Markings**

- **Polarity (Dipped Tantalum):** Dipped tantalum capacitors are strictly polarized. Polarity is indicated by a printed plus sign (+) or a small vertical stripe near the anode terminal. The anode (+) lead wire is manufactured noticeably longer than the cathode lead.
- **Non-Polarized Markings (Ceramic/Mica/Film):** These variations are non-polarized. They use a 3-digit numerical EIA code ("104" representing 100,000pF or 0.1uF) followed by a single capitalized letter denoting the manufacturing tolerance rating (J = ±5%, K = ±10%).

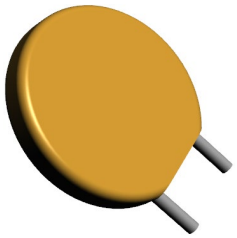
- **Voltage and Voltage Lines:** Rated operating voltages (50V, 1KV) are printed directly under the capacitance value code.

**Lead Form and Footprint Characteristics**

- **Lead Pitch Spacing:** The parallel leads typically exit the base with a standardized pitch grid spacing of 2.54 mm or 5.08 mm.
- **Crimped / Kinked Leads:** The wire terminal leads frequently feature factory-formed kinks or offsets right beneath the resin body. These crimps act as mechanical standoffs, preventing the uneven resin bead from seating inside the PCB through-holes, ensuring a level assembly and proper gas venting during automated wave soldering.

## 25.2.2 – Disk

**Disk:** A flat, circular, coin-like body. They resemble a small lollipop with two thin, parallel wire leads extending from the bottom edge of the disk.



Outer Coating and Texture

- **The Body:** Features a flat, rigid, wafer-thin circular profile. The edges are rounded but the face is completely flat to allow for easy part-number printing.
- **Material Coating:** Encapsulated in a matte, brittle ceramic or epoxy coating. The texture is slightly rough, powdery, or chalky to the touch, unlike the glossy finish of dipped capacitors.
- **Colors:** They are overwhelmingly manufactured in bright orange, tan, dark brown, or sky blue.

**Lead and Structural Features**

- Parallel Leads: Two solid, unshielded wire leads protrude from the bottom edge of the circle.
- **Non-Polarized:** The component is non-polarized. Both leads are manufactured to the exact same length, and the part can be inserted into a PCB in either direction.
- **Resin Incursion:** The ceramic coating often bleeds slightly down onto the tops of the metal leads. To prevent short circuits or seating issues, the leads are frequently formed with a kink or hockey-stick bend to keep the coated section safely above the PCB surface.

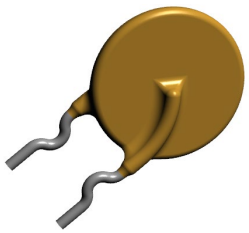
**Typical Markings and Identification**

Because the body is flat, information is stamped cleanly across one or both faces using high-contrast black or white ink:

- **Capacitance Code:** Uses a three-digit EIA code. The first two digits are the value, and the third is the multiplier in picofarads (103 equals 10,000pF or 0.01uF).
- **Tolerance Letter:** A single letter follows the digits (K = ±10%, M = ±20%), Z = +80% -20%).
- **Voltage Rating:** Clear numeric stamps designate the maximum voltage threshold (50V, 1KV, or 2KV). High-voltage disk capacitors are significantly thicker and larger in diameter.

## 25.2.3 – Disk With Offset Leads

**Disk With Offset Leads:** An "out-side kink" or "formed lead" disk capacitor) features the same flat, coin-shaped body as a standard disk capacitor, but its parallel wire leads are mechanically bent outward immediately below the resin coating before dropping vertically into the board. This built-in structural modification is specifically designed to wider the lead spacing and mechanically lock the component onto a printed circuit board (PCB).



**The Offset Lead Geometry**

- **The "Hockey Stick" or "Kink" Bend:** The two wire leads emerge from the circular base close together, flare outward sharply at an angle, and then bend straight down again. This creates a distinct "Z" or hockey-stick shape on each lead.
- **Lead Pitch Widening:** The primary physical purpose of this offset is to expand the spacing between the wires. For example, it often stretches a narrow 2.54 mm body exit spacing out to a wider, standard 5.05 mm footprint pitch on the PCB.
- **Mechanical Standoff:** The horizontal section of the bent wire acts as a built-in shelf. This shelf physically prevents the capacitor body from sliding too deep into the PCB through-holes.

**Body Coating and Resin Control**

- **Resin Incursion Prevention:** On standard straight-lead disk capacitors, the brittle coating material often bleeds unpredictably down the leads. The sharp offset bend acts as a physical barrier that stops this non-solderable resin coating from reaching the solder pads.

- **Stable Seating:** Because the bends rest perfectly flat against the top surface of the circuit board, they ensure the flat, circular disk stands perfectly upright and uniform across production lines.

**Identification, Texture, and Sizing**

- **Symmetry:** While the leads are bent outward, the offsets are perfectly symmetrical. Because ceramic disk capacitors are non-polarized, the component remains completely bi-directional.
- **Physical Profile:** The outer casing retains its signature matte, slightly chalky ceramic finish – typically in bright orange, tan, or safety-certified blue.
- **High-Voltage Variants:** Safety capacitors (X/Y class) and high-voltage disks heavily utilize offset leads to maximize the physical distance between the bare wires, preventing electrical arcing across the surface of the PCB.

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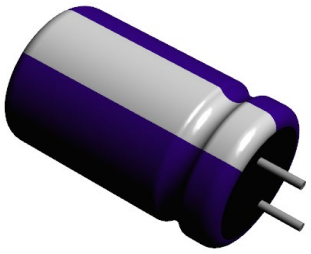
## 25.2.4 – Electrolytic

**Electrolytic:** Upright, metallic, cylindrical canister design. Unlike ceramic capacitors, these parts are strictly polarized and hold much higher capacitance values, making them a staple for power filtering on printed circuit boards.



**Through-Hole (Radial) Type:** Through-hole variations stand tall on the board like miniature silos. Their structure includes:

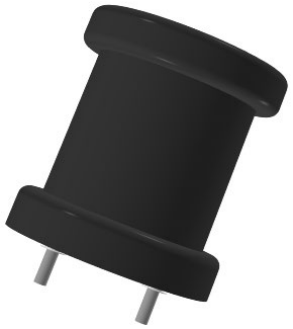
- **The Can:** An aluminum cylinder wrapped in a tight plastic insulating sleeve (usually colored black, dark blue, green, or brown) with technical specifications printed in high-contrast text.
- **The Rubber Bung:** The bottom of the aluminum can is sealed with a dense, black rubber plug. Both wire leads pierce through this bung to exit parallel out of the base.**Unequal Leads:** To prevent reverse insertion, the positive lead (anode) is visibly longer than the negative lead (cathode).

**Key Visual and Safety Markings:** Regardless of the mounting style, specific markings ensure safety and proper layout alignment:

- **The Polarity Stripe:** A thick, vertical, contrasting band runs down the full height of the outer plastic wrap. This stripe features repeated minus symbols (–) to explicitly identify the negative lead directly beneath it.
- **The Safety Vent:** The top face of the aluminum cylinder features a distinct stamped groove pattern (typically an "X", "Y", or "+" shape). If the capacitor fails or overheats, this score line acts as a pressure relief vent, splitting open cleanly to release gas safely rather than exploding violently.
- **Explicit Ratings:** Text stamped on the body clearly states the maximum temperature rating (typically 85°C or 105°C), the direct capacitance value in microfarads (uF), and the working voltage threshold (16V, 25V, 50V)

## 25.2.5 – Inductor

**Inductor:** A through-hole component easily recognized by its exposed wire coil structure or a characteristic hour-glass drum body enclosed in heat-shrink tubing. Unlike multi-terminal transformers, it features exactly two parallel conductive wire leads protruding downward from its base, allowing it to stand vertically to minimize its PCB footprint.



**Common Physical Forms**

- **Unshielded Drum / Bobbin Inductor:** The most recognizable type features a distinct dumbbell or hourglass-shaped ferrite core wrapped in tightly wound enameled copper wire. The entire cylinder is encased in a protective matte-black or colored polyolefin heat-shrink sleeve, giving it a textured, slightly rubbery look with a dimple or taper in the middle.
- **Toroidal Radial Inductor:** Features a doughnut-shaped ferrite ring with thick enameled wire coiled around its entire radius. To mount radially, the two wire ends terminate downward. Larger units are glued or mechanically fastened down to a small flat square or rectangular plastic structural base tray equipped with fixed metal pins to ensure stable mounting.
- **Shielded Radial Inductor:** Designed to prevent electromagnetic interference (EMI), this style encapsulates the internal coil in a rigid, completely smooth molded plastic or ferrite cylinder housing. The top face is perfectly flat, and the entire assembly resembles a miniaturized, boxier version of an aluminum electrolytic capacitor but without any safety vent stamps.

**Geometry and Lead Features**

- **The Body:** Typically a squat, thick cylinder where the height is often roughly equal to or slightly greater than the diameter (6 x 8 mm or 8 x 10 mm sizes).
- **The Leads:** Two stiff, uninsulated tinned copper wires extend from the flat bottom base. Because inductors are non-polarized components, both leads are cut to the exact same length and can be soldered onto the PCB in either direction.
- **Lead Separation (Pitch):** The parallel wires exit the base with standardized, wide industrial grids commonly 5.08 mm or 7.50 mm to safely accommodate thicker high-current wire.

**Core Markings and Values**

- **Numeric Code Stamps:** The flat top surface of the heat-shrink sleeve or plastic casing is often printed with a white or silver 3-digit marking code denoting the value in microhenries (uH). For example, 221 translates to 220uH, and 102 denotes 1,000uH (1mH).
- **Tolerance Designator:** A capitalized letter frequently follows the three digits to specify structural tolerance (J = ±5%, K = ±10%, L = ±15%).

## 25.2.6 – Molded

**25.2.6 Molded:** A through-hole electronic component housing where the active or passive device is encapsulated in a rigid, precision-molded plastic or epoxy shell with all leads exiting from a single flat surface.

Unlike the irregular, bulbous shape of "dipped" components, molded bodies are formed using high-pressure injection molding. This process creates crisp, geometric shapes with uniform dimensions optimized for automated pick-and-place machines and robotic PCB assembly.

**Common Body Shapes and Geometry:** Molded body packages are engineered to standard industrial dimensions and generally fall into three geometric profiles:

- **Molded Box / Rectangular:** A perfect rectangular cuboid (often called a "box" package). The walls are flat, smooth, and meet at sharp 90° angles, common for film capacitors and specialized resistors.
- **Molded Cylinder:** A perfectly straight, rigid plastic column with a flat top and a flat bottom base, often used for molded inductors or specialized diodes.
- **Molded Tear-Drop / Wedge:** A smooth, uniform block that tapers slightly toward the top, typical for modern molded solid tantalum capacitors.

**Core Material and Texture**

- **The Shell:** Made of a hard, brittle, thermosetting plastic or epoxy resin (frequently glass-fiber reinforced).
- **Texture:** The surface is completely uniform, matte or semi-glossy, and entirely free of the liquid runs or droplet beads found on dipped components.
- **Colors:** They are overwhelmingly molded in deep matte black, dark grey, or vibrant red/box-car yellow (highly characteristic of specialized film capacitors).

**Lead Configuration and Base Features**

- **Parallel Pins:** Solid, rigid tinned copper or alloy leads protrude straight down from the flat bottom surface.
- **Built-in Standoff Feet:** The molded plastic base often features small, integrated molded bumps or ridges (bosses). These tiny feet lift the main component body roughly 0.50 mm off the PCB surface. This gap ensures that flux and solder gases can escape cleanly during wave soldering and allows cleaning solvents to pass underneath.
- **Lead Pitch Grid:** Leads are spaced at highly precise, standardized intervals – typically 2.54 mm, 5.08 mm, or 7.50 mm – matching standard PCB CAD layout grids exactly.

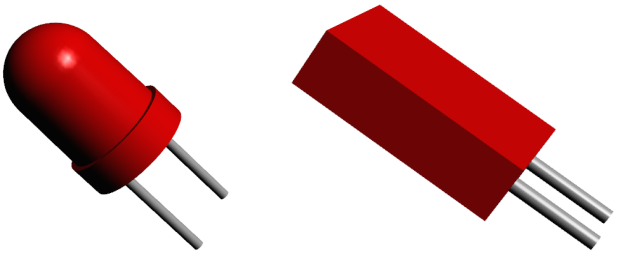
**Component Markings and Alignment:** Because the faces of a molded body are perfectly flat, technical details are clearly printed or laser-etched onto the top or broad side:

- **Polarity Keying:** For polarized components (like molded radial tantalum capacitors), a beveled/chamfered edge is molded into the top corner corresponding to the positive (+) lead, often accompanied by a printed laser stripe. Non-polarized versions (like film capacitors) feature perfectly symmetrical square corners.
- **Laser Etching:** Text including the manufacturer's logo, part series, capacitance/inductance values, and voltage ratings are permanently etched with high precision, ensuring readability even on tiny components.

## 25.2.7 – LED

**LED:** A polarized optoelectronic component easily recognized by its clear or tinted dome-shaped plastic body and two parallel wire leads extending from its base. It stands vertically on a printed circuit board (PCB) to project light upward or outward.

Depending on the application, they are manufactured in standard sizes like 3 mm (T-1), 5 mm (T-1 ¾), and 10 mm, all sharing a highly standardized physical profile.



**The Optical Body Geometry**

- **Body Shapes:** Round or Rectangle
- **The Epoxy Lens:** The main body is a solid, rigid cylinder topped with a hemispherical dome that acts as a focusing lens. The plastic can be completely water-clear, diffused (milky), or color-tinted to match the LED's output light.
- **The Flat Edge (Cathode Indicator):** The most distinct mechanical feature of the circular base is a **prominent flat notch or shaved edge** on the plastic rim. This flat side always corresponds to the negative terminal (cathode).
- **The Base Flange:** A small, raised plastic ridge or rim runs around the very bottom of the cylinder, used by automated insertion machinery to grip the component during assembly.

**Lead Configuration and Anvil Anatomy:** Because LEDs are highly polarity-sensitive and will not illuminate if reversed, the package features three separate physical keys to differentiate the terminals:

| Feature | Anode (+) | Cathode (-) |
|---|---|---|
| **Lead Length** | Noticeably Longer | Shorter |
| **Plastic Body** | Rounded side | Flat / Shaved side |
| **Internal Frame** | Smaller post (Pin) | Triangular block |

**Interior Construction (Visible Profile):** When looking through a clear or translucent LED body, you can see the internal lead-frame:

- **The Anvil:** The negative lead connects to a wide, flat triangular frame. The tiny semiconductor LED die sits inside a reflective cavity on top of this anvil.
- **The Post & Wire Bond:** The positive lead extends up as a thin post. A microscopic gold wire bonds the top of this post to the semiconductor die resting on the anvil.

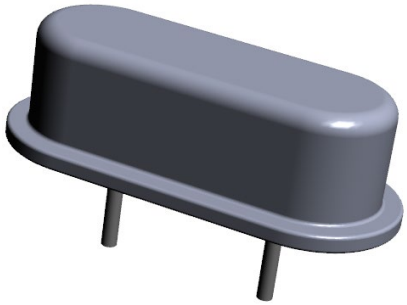
**PCB Mounting Variations**

- **Standard Vertical Mount:** The leads go straight into the PCB, resting the flange flush against the board or slightly elevated on a plastic spacer to ensure perfect alignment.
- **Right-Angle Mount:** The leads are bent 90° right below the plastic base (often encased in a black plastic housing block) so the dome lens points horizontally toward the edge of the enclosure to serve as an indicator light.

## 25.3 – Crystal (HC49)

Crystal (HC49): A radial, passive quartz resonator housed in a distinct metallic, capsule-like canister. It features an elongated, oval-profile body with two stiff wire leads exiting from a hermetically sealed glass base.

Commonly used to generate reliable reference clock frequencies for microcontrollers, it stands upright or lies flat against a printed circuit board (PCB).



**Standard Profiles (HC49/U vs. HC49/S):** The term "HC49" encompasses two primary height profiles that share identical footprint spacings but dictate vertical clearance:

- **Full-Height (HC49/U):** The traditional, tall profile. The metal body stands roughly 13.20 mm to 13.50 mm high, mimicking a tall metal silo on the circuit board.
- **Low-Profile / Half-Height (HC49/S or HC49/US):** The modern, horizontally squashed equivalent. It restricts the package height to a compact 3.50 mm to 4.20 mm, preventing interference with stacked shield boards or tight enclosures.

**Physical Dimensions and Structure**

- **The Metallic Can:** Constructed from nickel-plated or tin-plated steel, providing rugged structural armor and vital electromagnetic shielding against radio-frequency noise.
- **Oval Cross-Section:** The body footprint is a distinct flattened oval (stadium shape) measuring roughly 11.40 mm to 11.50 mm in length and 4.70 mm in width.
- **The Resistance-Weld Flange:** A prominent, sharp metal lip or rim projects outward around the lower edge where the cap joins the header. This flange seals the internal quartz crystal wafer in a pure vacuum or dry nitrogen environment.

**Base Elements and Lead Configuration**

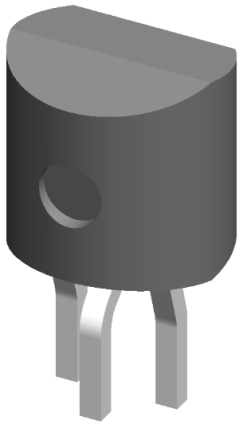
- **Glass-to-Metal Seal:** The base of the container features a flat metal header with two tiny glass eyelets. These glass beads insulate the conductive pins from the metal canister while maintaining the airtight seal.
- **Symmetrical Radial Leads:** Two rigid, uninsulated tinned copper wires pass through the glass seals to extend parallel down into the board. Crystals are non-polarized components, meaning the leads are identical in length and can be installed facing either direction.
- **Lead Spacing (Pitch):** The center-to-center lead spacing is highly precise, fixed at a standardized 4.88 mm pitch grid.

**Mechanical Mounting Variants:** Due to its heavy metallic shell, mounting requires distinct configurations based on vibration limits and height profiles:

- **Vertical Stand-Up (Standard):** The pins slide directly through the PCB holes, dropping the resistance-weld lip right over the copper traces.
- **Horizontal Lay-Down:** In space-constrained layouts or high-vibration applications, a tall HC49/U can is often bent 90° horizontally. It is laid flat against the board surface and anchored with a dollop of adhesive or a small mechanical metal strap soldered to a ground trace.
- **The Mylar Spacer Pad:** Because the entire outer canister is metallic and conductive, components are frequently supplied with a thin, pre-installed plastic or Mylar insulating spacer resting over the pins against the base. This prevents the metal body from causing unexpected electrical short-circuits across bare board traces routed directly beneath the crystal.

## 25.4 – TO-92

**TO-92:** A highly ubiquitous, low-cost through-hole radial plastic package most commonly used for low-power transistors, voltage regulators, and signal sensors. It is instantly recognizable by its compact, semi-cylindrical, "D-shaped" body with three distinct parallel wire leads emerging from its base.



**JEDEC**: TO-226

**Geometric Body Anatomy**

- **The "D-Shape" Profile:** If viewed from directly above, the plastic body forms a distinct capital letter "D". It features one perfectly flat front face and a smoothly rounded, semi-circular back wall.
- **The Plastic Shell:** The encapsulation consists of a hard, rigid, matte-black epoxy compound that protects the sensitive internal silicon semiconductor die from moisture and physical damage.
- **Compact Dimensions:** It is a small package, typically measuring roughly 4.50 mm to 5 mm in height, with a width and depth of about 4 mm to 5 mm.

**Lead Configuration and Lead Formats:** The TO-92 traditionally features three solid, uninsulated tinned alloy leads protruding straight down from the flat bottom base. Depending on production needs, these leads are shipped in two common layout styles:

- **Straight Inline Leads (TO-92 Bulk):** All three pins exit in a tight, perfectly straight line with a very narrow center-to-center pitch of just 1.27 mm.
- **Spread / Bent Leads (TO-92 Tape & Reel):** For automated insertion and to reduce solder-bridging short circuits, the middle lead stays straight while the two outer leads flare outward. This transforms the tight line into a wider, triangular triangular arrangement with a standard 2.54 mm grid pitch.

**Pin Identification and Markings**

- **Laser-Etched Front Face:** Part numbers (such as 2N3904 or LM78L05) along with manufacturer logos and batch codes are laser-etched directly onto the flat face of the "D" shape.
- **Strict Pin Orientation:** Pin ordering is asymmetrical and highly critical. When holding the package at eye level with the flat face directly facing you and the leads pointing downward, the pins are counted from left to right as Pin 1, Pin 2, and Pin 3.
- For standard Bipolar Junction Transistors (BJTs), this sequence typically maps to Emitter-Base-Collector (E-B-C) or Source-Gate-Drain (S-G-D), depending on the specific part registry.

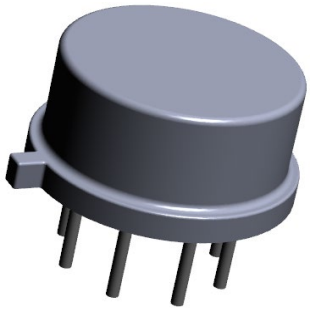
**PCB Layout and Assembly Realities**

- **Silkscreen Alignment:** The PCB silkscreen outline for a TO-92 is drawn as a clear "D" shape to show the assembler which way the flat face must point, preventing catastrophic reverse installation.
- **Thermal Limitations:** Because the package is entirely plastic and lacks a dedicated metal cooling tab (unlike the larger TO-220), it relies solely on the surrounding air and its thin wire leads to shed heat. It is strictly limited to low-power applications, typically under 1 Watt.

## 25.5 – TO Cylindrical Style

**TO Cylindrical Style:** A highly durable, hermetically sealed through-hole component casing. The "TO" stands for Transistor Outline, and these cylindrical variants represent some of the earliest and most robust designs in semiconductor packaging history.

They are widely used for precision small-signal transistors (like the classic Central Semiconductor 2N2222A), operational amplifiers, legacy integrated circuits, and optoelectronic sensors.



**JEDEC**: MO-002, MO-006, TO-205, TO-206

**Core Geometry and Construction**

- **The Metal Can Cap:** The component is enclosed in a perfectly smooth, unpainted cylindrical shell made of nickel-plated steel, aluminum, or Kovar. This cap acts as an integrated Faraday cage, providing exceptional electromagnetic interference (EMI) shielding.
- **The Header Base Plate:** The bottom of the package is a flat, thick metal disc (the header). The internal silicon semiconductor die is mounted directly onto this base plate for rigid mechanical support.
- **Glass-to-Metal Seals:** To prevent short-circuits, the metal leads pass through the header via individual, tiny beads of insulated glass. These beads are fused under extreme heat, maintaining an airtight (hermetic) vacuum or nitrogen-filled chamber inside the can to shield the die from atmospheric moisture and contaminants.

- **Common Size Variants:** Cylindrical TO packages share the same design language but scale drastically depending on pin counts and heat dissipation needs:
- **TO-18:** The smallest standard metal can, measuring roughly 4.70 mm to 5.40 mm in diameter. It usually features 3 leads arranged in a tight circular cluster and is the premium, rugged alternative to the plastic TO-92 package.
- **TO-5 / TO-39:** A medium-sized cylinder with a base diameter of approximately 8.90 mm. While TO-39 typically features 3 pins for medium-power transistors, the TO-5 header can house anywhere from 2 up to 10 pins arranged in a circular array, commonly used for vintage multi-pin op-amps.
- **TO-8:** A much larger, flat cylindrical format designed to handle higher operational power and internal circuitry, often housing multi-pin micro-sensors or hybrid modules.
- **Pin Orientation and The Alignment Tab:** Because the package is perfectly circular, it requires a physical feature to indicate pin assignments:
- **The Indexing Tab:** A tiny, sharp metal tongue or ridge projects outward from the bottom rim of the header base plate.
- **Pin 1 Identification:** When looking directly at the bottom base of the package with the leads pointing at your face, the indexing tab is used as the orientation key. The pin positioned immediately clockwise from the tab is Pin 1 (frequently the Emitter on standard 3-pin transistors). The rest of the pins are numbered sequentially following a clockwise circle.
- **Case Grounding:** In many RF and high-frequency applications, one specific pin is welded directly to the metal header base plate instead of passing through an insulating glass bead, automatically grounding the metal outer shield to the PCB ground plane.

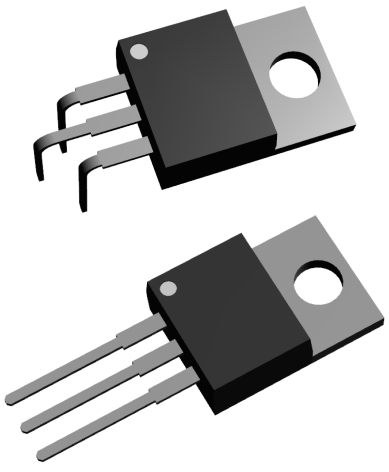
**PCB Footprint and Mounting Styles**

- **The Pin Circle Array:** On a circuit board, the through-hole landing pads are arranged in a perfect circular pitch layout rather than a straight line. For instance, a TO-18 typically uses a 2.54 mm diameter pin circle, while a TO-5 expands to a 5.08 mm pin circle.
- **Lead Splaying:** Because the circular pin pattern is so compact, assembly technicians or automated machines often flare the leads outward into a wider triangular configuration before dropping them into the PCB to prevent solder bridges.
- **Silkscreen Target:** The PCB silkscreen outline mimics a circle with a tiny notch on the perimeter, matching the layout of the physical orientation tab exactly to avoid reverse insertion.

## 25.6 – Flange Mount (TO) Horizontal & Vertical

**Flange Mount (TO) Horizontal & Vertical Mount:** A high-power semiconductor housing designed with a built-in mechanical metal tab, wing, or extended base (the flange). The primary purpose of this design is to allow the component to be rigidly bolted or clamped directly to an external heatsink or metal chassis, optimizing thermal transfer for components generating high waste heat.

The "TO" designation stands for Transistor Outline, and flange mount variants bridge the gap between delicate board circuitry and heavy-duty mechanical thermal management. They are split into two primary design families: Tabbed In-line Packages and Diamond/Flange Base Packages.



**JEDEC**

(Vertical): MO-048, MO-168, MO-218, TO-247
(Horizontal): TO-220, TO-254, TO-257, TO-267

**Tabbed In-line Family (TO-220, TO-247):** The most modern and common type of flange mount, where the component stands vertically or lies flat on the board:

- **The Tab Flange:** A prominent, flat **exposed metal tab** extends from the top or back of the rectangular plastic body. It features a single, centralized **mounting hole** (typically sized for a #4-40 or M3 screw).
- **Electrical Caveat:** The metal tab is typically an expansion of the internal lead frame and is electrically live (usually tied to the Center Pin / Collector / Drain).
- **Variations (Full-Pack):** Isolated variations, such as the **TO-220FP**, encase the metal flange entirely in a thin layer of over-molded plastic. This eliminates the need for an external mica insulator during installation, though it reduces thermal efficiency slightly.

**Diamond / Metal Plate Family (TO-3):** A legacy, heavy-duty "metal can" package designed for extreme current and rugged reliability:

- **The Diamond Flange:** The base of the package is a thick, rigid diamond-shaped metal plate. It features two mounting holes positioned on opposite wings along the long diagonal line of the diamond.
- **The Cap:** A cylindrical metal hat is welded to the center of the diamond plate, protecting the silicon die in a hermetic vacuum.
- **Body as a Terminal:** Only two pins (typically Base and Emitter) protrude through glass seals on the bottom. The massive metal flange body *is* the third electrical connection (the Collector), requiring the mounting screws themselves to pass current to the PCB traces via eyelet lugs.

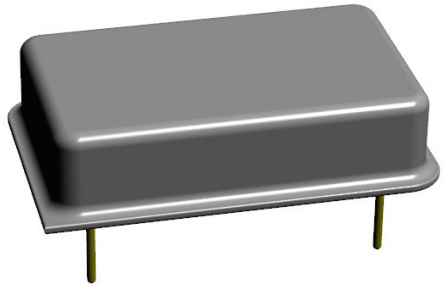
**Mechanical Installation Realities:** Because flange mount packages are mechanically fastened, their physical footprint layout requires strict adherence to assembly guidelines:

- **Thermal Interface Materials (TIM):** To prevent electrical short-circuits to a grounded heatsink, the flange is often sandwiched between a silicone/mica insulating pad and a plastic insulating shoulder washer inserted inside the screw hole. Thermal grease is applied to fill microscopic air gaps.
- **Lead Stress Prevention:** When bending the pins of a TO-220 to mount it flat against a board, the leads must be clamped tightly *before* the bend is made. Bending forces must never pull against the plastic body, or the internal wire bonds will break.
- **Torque Control:** Screws must be tightened to specific torque limits (roughly 0.5 to 0.8 N) for a TO-220). Excessive torque will warp the flat metal flange, causing it to bow upward and lose thermal contact with the heatsink.

## 25.8 – Oscillator

**Oscillator:** A through-hole radial lead crystal oscillator (commonly called a clock oscillator or active crystal) is a fully self-contained timing circuit housed in a metallic, rectangular canister with exactly four parallel pins protruding from its base.

Unlike passive 2-pin quartz crystals that require external capacitors and inverter circuits to function, active oscillators combine the quartz wafer, a built-in oscillation circuit, and load capacitors into a single powered module. They stand vertically on a printed circuit board (PCB) to feed a clean, pre-stabilized square-wave clock signal directly into microprocessors.



**Standard Geometric Profiles:** Through-hole active oscillators are built around legacy Dual In-line Package (DIP) footprints. Although they only possess 4 pins, their metal cans span the exact outer dimensions of standard 8-pin or 14-pin integrated circuits:

- **Full-Size (DIP-14 Package):** A long, distinct rectangular block mimicking a 14-pin chip footprint. Standard dimensions are roughly 20.40 mm x 12.90 mm with a height of 5.5mm.
- **Half-Size (DIP-8 Package):** A compact, perfectly square variant mimicking an 8-pin chip footprint. Standard dimensions are roughly 12.70 mm x 12.70 mm with a height of 5.50 mm.

**Canister Shell Construction**

- **Hermetically Sealed Can:** The body consists of a nickel-plated or tin-plated steel cover. It is resistance-welded to a flat metal header plate, shielding the fragile internal micro-circuit from environmental humidity and electromagnetic interference (EMI).

- **Rounded and Sharp Geometry:** The upper edges of the metallic shell are smoothly rounded, but one specific corner on the base is manufactured with a sharp 90° angle or index dot to serve as a visual key for orientation.

**Pin Layout and Identification (The "Missing Pins" Phenomenon):** Even though the metal enclosure matches a standard 8-pin or 14-pin IC frame, only four physical corner leads are present. The empty spaces where intermediate pins would normally be completely smooth and sealed off.

When looking directly at the **top face** of the oscillator with the sharp/indexed corner oriented at the bottom-left, the active pins drop into the layout grid as follows:

| Pin Designation | Full-Size (DIP-14) Location | Half-Size (DIP-8) Location |
|---|---|---|
| Pin 1 | Bottom-Left Corner | Bottom-Left Corner |
| Pin 7 / 4 | Bottom-Right Corner (Pin 7) | Bottom-Right Corner (Pin 4) |
| Pin 8 / 5 | Top-Right Corner (Pin 8) | Top-Right Corner (Pin 5) |
| Pin 14 / 8 | Top-Left Corner (Pin 14) | Top-Left Corner (Pin 8) |

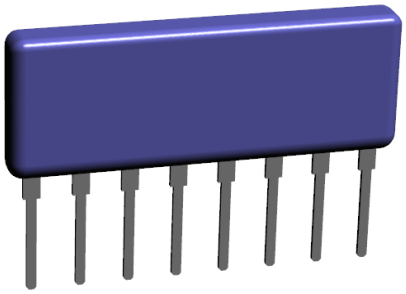
**PCB Footprint and Installation Characteristics**

- **Lead Pitch:** The four corner pins maintain standard DIP spacing. Row-to-row spacing is 7.62 mm, while side-to-side pin spacing spans either 15.25 mm for Full-Size or 7.62 mm for Half-Size.
- **Glass-to-Metal Insulation:** The pins protrude out of the flat metal bottom plate through microscopic, insulating glass beads.
- **Case Grounding:** To minimize radio-frequency radiation, Pin 7 (or Pin 4 on half-size) is intentionally welded directly to the interior metal header wall. This structural link automatically connects the massive metal outer shield directly to the PCB ground plane when soldered.

## 25.9 – Single In-Line Package (SIP)

**Single In-Line Package (SIP):** a flat, rectangular, wafer-thin body with a single row of straight conductive pins protruding from its bottom edge.

Because it stands perfectly upright – like a small fence on the printed circuit board – it is highly favored for space-constrained layouts. It is most commonly used for resistor networks, legacy memory modules (SIMMs), diodes, and low-power power management modules.



**JEDEC**: MO-068

**Geometric Profile and Texture**

- **The Body:** Features an elongated, narrow rectangular profile. It has a very small depth (thickness) relative to its length and height, maximizing available board space.
- **Material Encapsulation:** Typically constructed from a rigid, matte-black thermosetting plastic or a smooth molded epoxy resin.
- **Profiles:** They exist in low-profile, medium, and high-profile configurations depending on the internal circuitry, ranging from 4 mm to 12 mm in total height.

**Lead Arrangement and Pitch**

- **The Single Row:** Unlike a Dual In-line Package (DIP) which uses two parallel rows of legs, a SIP features exactly one straight line of parallel metal pins.
- **Pin Count Variability:** A SIP can have anywhere from 2 to over 40 pins along its single axis, though 4-pin to 10-pin variants are the most common in standard commercial hardware.
- **Standardized Grid Pitch:** The center-to-center pin spacing is manufactured to a highly precise, industry-standard 2.54 mm linear pitch, perfectly matching the

default grid lines of standard prototyping breadboards and CAD software.

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**Pin Identification and Keying**

Because a single row of pins can easily be accidentally flipped 180° during manual assembly, the package features distinct visual orientation keys:

- **The Indexing Dot / Chamfer:** A molded recess dot, a printed stripe, or a beveled corner is placed on the body directly adjacent to Pin 1.
- **Pin Numbering:** Pin assignment is counted sequentially in a straight line from left to right (Pin 1, 2, 3, 4...) when viewing the front printed face of the component with the leads pointing downward.
- **Common Pin (Resistor Networks):** In bussed resistor networks, Pin 1 acts as the "Common" connection point for all internal resistors, while the remaining pins connect to individual resistors.

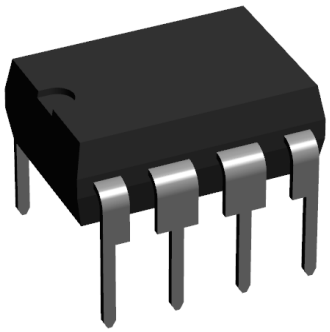
**PCB Mechanical Realities**

- **High Structural Leverage:** Because SIPs stand tall on a single narrow line of legs, they are highly vulnerable to physical impacts, vibration, and tipping during wave soldering.
- **Standoff Bumps:** The base of the plastic housing often features tiny, built-in molded spacer feet to keep the body slightly raised above the board. This gap ensures solder gases can escape and cleaning chemicals can wash away any residual manufacturing flux.
- **The Zig-Zag Variant (ZIP):** To achieve even higher density, some packages utilize a Zig-zag In-line Package (ZIP) lead form, where the pins alternate bending slightly forward and backward, transforming the single row into a staggered, dual-line footprint on the PCB.

## 25.10 – Dual In-Line Package (DIP)

**Dual In-Line Package (DIP):** A rectangular housing with two parallel rows of downward-pointing conductive pins protruding from its longer sides.

Widely used for integrated circuits (ICs), microcontrollers, operational amplifiers, and optocouplers, its design resembles a mechanical "bug" or "centipede" standing over the printed circuit board (PCB).



**JEDEC**: MO-001, MO-015, MO-016, MO-024, MO-036, MO-037, MO-038, MO-039, MO-043, MO-095, MO-103, MO-122, MS-001, MS-010, MS-011, MS-015, MS-019, MS-020, MS-021, MS-030, MS-031, MS-032

**Geometric Profile and Construction**

- **The Body:** A rigid, elongated rectangular block. The most standard version is a Plastic DIP (PDIP) molded from a matte-black thermosetting epoxy. For high-reliability, aerospace, or vintage military gear, a Ceramic DIP (CDIP) is used, recognizable by its smooth, chalky purple-grey or white body.
- **The Two Lead Rows:** Pins emerge horizontally from both long sides of the body before bending sharply 90° downward. This creates two identical, parallel rows of legs flanking the main chip housing.
- **Inward Lead Flare:** Before soldering, the legs flare outward at a slight angle (8° to 15°) so they act like springs. This flair holds the chip firmly inside the PCB through-holes during manufacturing, so it does not fall out before reaching the soldering machine.

**Standard Sizing and Pitch Dimensions:** DIP spacing adheres to rigid JEDEC industry standards to guarantee compatibility with prototyping breadboards and standard IC sockets:

- **Linear Pin Pitch:** The center-to-center distance between individual pins along a single row is exactly 2.54 mm.
- **Row-to-Row Spacing:** The width between the two rows of legs scales based on the size of the chip:
  - **Narrow DIP (7.62 mm):** The standard for small chips ranging from 8 pins up to 28 pins.
  - **Wide DIP (15.24 mm):** Used for large, dense integrated circuits ranging from 24 pins up to 64 pins.
  - **Skinny DIP (10.60 mm):** A rare, intermediate hybrid width used on specialized memory chips.

**Orientation Keys and Pin Numbering Protocol:** Because reversing an integrated circuit can instantly destroy it when powered up, the DIP standard enforces a strict physical layout keying system:

- **The Orientation Notch:** One of the two short, narrow ends of the rectangular body features a semi-circular notch or U-shaped indentation. On some smaller chips, this notch is replaced or supplemented by a small molded circular dot placed directly in the top corner next to Pin 1.
- **The Counter-Clockwise Counting Rule:** Pin numbering is determined relative to the notch. Place the chip flat in front of you so that the orientation notch is facing up (pointing away from you):
  - Pin 1 is the very first pin located at the top-left corner, immediately to the left of the notch.
  - Numbering proceeds straight down the left row sequentially (Pin 1, 2, 3, 4...).
  - Upon reaching the bottom of the left row, the numbering jumps across to the right side and wraps up the right row from bottom to top.
  - The highest-numbered pin on the chip will always sit at the top-right corner, directly across from Pin 1.

**PCB Assembly and Sockets**

- **Direct Soldering vs. Sockets:** DIP chips can be soldered directly into the PCB through-holes. However, they are frequently pushed into a plastic DIP IC Socket that has been pre-soldered to the board. This allows for quick, toolless replacement of a failed chip without risking thermal damage to the PCB traces from a desoldering iron.
- **Standoff Shoulders:** Each metal leg features a wider "shoulder" section right where it emerges from the plastic body. These shoulders act as physical stoppers, preventing the plastic housing from resting flush against the PCB. This leaves a critical air gap underneath for flux removal, cleaning solvents, and thermal air cooling.

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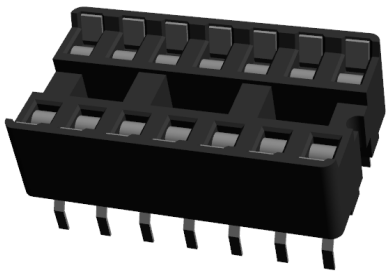
## 25.10 – Dual In-Line Package (DIP Socket)

**Dual In-Line Package (DIP Socket):** A specialized through-hole connector permanently soldered to a printed circuit board (PCB) to hold a DIP integrated circuit (IC) without soldering the chip itself. It mirrors the exact rectangular footprint, row spacing, and pin count of the specific DIP chip it is designed to accommodate, acting as an intermediary mechanical and electrical bridge. Depending on reliability requirements, they are manufactured in two primary styles: Stamped-Contact (Economy) and Machined-Contact (Turned-Pin/Premium).



**Structural Frame and Geometry**

- **The Body:** A rigid, ladder-like frame molded from black, glass-reinforced thermoplastic. It consists of two long outer parallel rails connected by one or more thin cross-beams (struts). This open, skeletal layout leaves the PCB surface underneath visible for routing traces or placing decoupling capacitors.
- **The Orientation Notch:** Like the ICs they hold, one short end of the socket frame features a molded U-shaped notch or indentation. This notch aligns perfectly with the chip's orientation key to ensure it is not inserted backwards.
- **Stand-off Feet:** The bottom of the plastic frame features small, molded-in spacer nubs. These lift the plastic body roughly 0.50 mm off the PCB, allowing manufacturing gases to escape during wave soldering and flux cleaning solvents to pass underneath.

**Dual Contact Technologies**

The top face of the socket rails features two rows of small entry holes containing hidden internal metal spring clips. These contacts grip the IC legs when the chip is pushed into the socket:

- **Stamped / Dual-Leaf Contacts (Economy):** The internal terminals are stamped from flat sheets of phosphor bronze or brass and plated with tin. They feature two flat, spring-loaded leaves that pinch the wide flat sides of the IC pin. While highly cost-effective, they are prone to losing tension over multiple insertions or loosening under heavy vibration.
- **Machined / Turned-Pin Contacts (Premium):** The contact outer shells are individually machined on high-precision lathes into solid, gold-plated or tin-plated cylindrical tubes. Inside each tube sits a stamped, multi-finger beryllium-copper spring clip (resembling an internal crown). These provide gas-tight electrical contact and maximum mechanical retention, making them the standard for aerospace, military, and high-vibration applications.

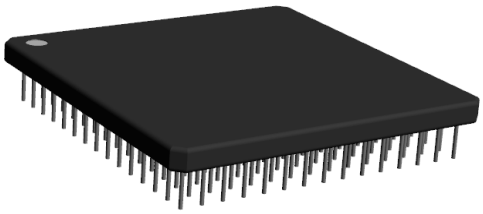
**Pin and Dimensional Matrix:** DIP sockets precisely duplicate the exact standardized pitch layout of JEDEC DIP standards to guarantee drop-in compatibility:

- **Linear Pin Pitch:** The center-to-center distance between adjacent entry holes down a single row is exactly 2.54 mm.
- **Row-to-Row Spacing (Width):** Sockets are manufactured in two standard industrial widths:
  - **7.62 mm:** For standard narrow chips (typically 8, 14, 16, 18, 20, 24, or 28 pins).
  - **15.24 mm:** For wide integrated circuits and microprocessors (typically 24, 28, 40, or 48 pins).
- **The PCB Pins:** Protruding out the bottom of the socket are solid, uninsulated tinned alloy pins. On stamped sockets, these pins are flat, rectangular tabs; on machined sockets, they are perfectly smooth, solid cylinders tapering to a point to slip effortlessly into PCB drill holes.

## 25.11 – Pin Grid Array (PGA)

**Pin Grid Array (PGA):** A high-pin-count, through-hole integrated circuit housing characterized by a square or rectangular body with a dense matrix (grid) of parallel conductive pins covering its entire bottom surface.

Unlike a DIP or SIP package where pins are restricted only to the outer edges, a PGA utilizes the complete floor space of the component base. This architecture allows it to route hundreds of electrical connections. It was the dominant package design for high-performance microprocessors (such as the Intel 80486 and early AMD Athlon/Phenom CPUs) before surface mount and Land Grid Array (LGA) formats took over.



**JEDEC**: MO-066, MO-067, MO-083, MO-145, MS-017

**Structural Materials and Anatomy**

- **The Carrier Body:** PGAs are traditionally square wafers built from one of two rigid materials:
- **Ceramic PGA (CPGA):** A heavy, chalky, multi-layer ceramic plate (often purple, white, or dark grey) topped with a shiny gold or silver metal heat-spreader cap. These offer premium thermal management and hermetic sealing.
- **Plastic PGA (PPGA):** A lighter, cost-effective alternative made from a dense organic polymer resin, often colored black or deep green.
- **The Pin Matrix:** The bottom face is populated by an array of thin, solid, gold-plated or tin-alloy pins protruding straight down. These pins are highly fragile and easily bent if mishandled.

**Grid Array Geometry and Keying**

- **The "Interstitial" Layout:** Pins are arranged in an even grid pattern, typically spaced at a standard linear pitch of 2.54 mm or a tighter 1.27 mm on denser, modern iterations.
- **The Center Void:** To save cost and leave space for the silicon die and internal decoupling capacitors, the center of the grid is almost always left empty (devoid of pins), creating a hollow square frame pattern.
- **Physical Orientation Keying:** Because reversing a high-power processor can immediately destroy it, PGAs enforce strict physical keying. One or more corners of the array will feature a missing pin, a staggered corner pin, or a beveled 45° corner on the plastic/ceramic package. This layout forces a single, correct installation alignment.

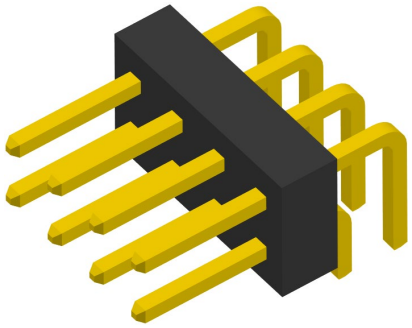
**PCB Installation and ZIF Sockets**

- **The ZIF Intermediary:** Due to the massive insertion force required to push hundreds of pins into a tight circuit board simultaneously, PGAs are rarely soldered directly into a PCB. Instead, they are dropped into a Zero Insertion Force (ZIF) Socket pre-soldered to the board.
- **The Locking Lever:** A ZIF socket features a small mechanical arm. When the arm is raised, the internal socket contacts open completely, allowing the PGA pins to drop in freely with zero resistance. Lowering and clamping the lever slides the internal socket matrix horizontally, firmly gripping every pin to establish a gas-tight electrical bond.

## 25.12 – Header, Right Angle Post

**Header, Right Angle Post:** a board-level connector featuring a single or multi-row array of rigid square metal pins bent at a sharp 90° angle.

This specific component is structurally engineered to allow multi-wire cables, daughterboard modules, or ribbon connectors to plug into the host printed circuit board (PCB) parallel to the board surface. It provides a low-profile connection that prevents wire strain and keeps vertical clearance to a minimum.



**The Pin Anatomy and the 90° Bend:** The component is built using solid, square-cut wire posts (typically made of brass or phosphor bronze) that are plated with tin or gold. Each pin is physically divided into three distinct segments by its bend:

- **The Solder Tail:** The shorter, vertical end of the pin that passes down through the PCB plated through-holes to be soldered on the underside of the board.
- **The Right-Angle Bend:** A precision factory-formed 90° corner situated immediately beneath the plastic insulator strip.
- **The Mating Post:** The longer, horizontal segment of the pin that projects outward past the edge of the PCB. This is the active terminal that slides into a mating female housing or jumper wire.

**The Plastic Insulator Strip (The "Backbone")**

- **Material Construction:** The pins are held uniformly in place by a narrow, rigid strip of high-temperature plastic (such as Nylon, PBT, or LCP) capable of withstanding the heat of wave soldering or manual rework.
- **Breakaway Design (Unshrouded):** On basic unshrouded versions, the plastic strip features small notches or score lines between each pin cavity. This allows assembly technicians to easily snap long 40-pin master strips down to any custom pin count needed (a 2-pin or 4-pin block) without specialized cutting tools.

**Array Variations and Matrix Configurations:** Right-angle post headers are highly modular and scale across standard layout configurations:

- **Single-Row (1xN):** A single line of parallel horizontal pins protruding from the plastic housing.
- **Dual-Row (2xN):** Two parallel lines of horizontal pins stacked vertically. The bottom row passes straight through the plastic into the PCB, while the upper row features longer vertical bends to step over the lower row, ensuring both sets of pins line up perfectly on the horizontal mating plane.
- **Multi-Row:** Stacking configurations up to 3 or 4 rows deep are utilized in high-density backplanes or legacy computing buses (3 x 40 arrays).

**Dimensional and Pitch Standards**

To maintain universal compatibility with external connector families, right-angle post headers are tightly tied to standardized industrial grids:

- **Pitch Spacing:** The center-to-center linear distance between pins is most commonly a standard 2.54 mm pitch. Denser, more compact electronics use sub-miniature pitches of 2.00 mm, 1.27 mm or even 1.00 mm.
- **Square Post Thickness:** In the dominant 2.54 mm family, each metal post is cut to a precise cross-sectional dimension of 0.64 mm square.

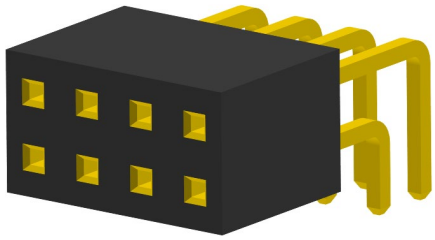
**Unshrouded vs. Shrouded Variations**

- **Unshrouded Headers:** The bare pins are completely exposed. This offers the lowest cost and smallest physical layout footprint but leaves the pins vulnerable to bending if bumped or mishandled.
- **Shrouded / Boxed Headers:** The plastic housing extends outward to create a rigid plastic box or wall around the mating posts. This shroud incorporates physical mating notches (polarization slots) to ensure an external wire harness can only be plugged in facing the correct direction, preventing catastrophic reverse-voltage connections.

# 25.13 – Header, Right Angle Receptacle

**Header, Right Angle Receptacle:** A right-angle female header or socket strip) is a board-level connector featuring a single or multi-row plastic housing filled with internal spring contacts and pins bent at a sharp 90° angle.

While a post header features exposed male pins, a receptacle header contains recessed female entry holes. This design allows a daughterboard or a male pin wire harness to plug directly into the host printed circuit board (PCB) parallel to the board surface, keeping vertical overhead clearance to an absolute minimum.



**Geometric Profile and Structural Features**

- **The Connector Body:** A long, rigid rectangular block molded from a high-temperature thermoplastic (such as Nylon or PBT). The front-facing edge contains a row of tiny, square entry ports to receive male pins, while the back or bottom edge is sealed.
- **The Right-Angle Solder Tails:** Stiff metal pins emerge from the back of the plastic housing, bend sharply 90° downward, and pass vertically into the PCB plated through-holes.
- **Flush or Edge Mounting:** The plastic body rests flat on the board surface, often positioned right along the physical edge of the PCB so an external device can slide horizontally into the assembly.

**Internal Contact Architecture**

- **Dual-Leaf Spring Contacts:** Inside each plastic entry port sits a hidden, stamped metal terminal made of phosphor bronze or brass, heavily plated with gold or tin.
- **Wiping Action:** These internal contacts act like tiny tuning forks or spring clamps. When a male pin enters the socket, it pushes these leaf springs apart. This mechanical pressure ensures a constant, low-resistance, vibration-resistant electrical connection.

**Dimensional Matrix and Pitch Standards:** Receptacle headers are engineered to perfectly mirror standard male pin layout dimensions:

- **Standard Linear Pitch:** The center-to-center spacing between the internal socket cavities is most commonly an industry-standard 2.54 mm. More compact systems feature tighter sub-miniature grids like 2.00 mm or 1.27 mm.
- **Mating Compatibility:** In the standard 2.54 mm pitch family, the internal sockets are precision-sized to accept standard 0.64 mm square male posts.

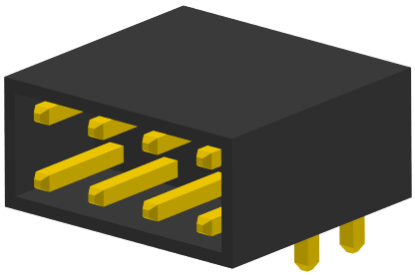
**Array Configurations**

- **Single-Row (1xN):** A single horizontal line of entry sockets running parallel to the circuit board.
- **Dual-Row (2xN):** Two horizontal rows of entry sockets stacked vertically. To translate this into a PCB footprint, the pins from the upper row are manufactured with longer, stepped 90° legs that jump over the lower row's pins, creating two distinct, staggered rows of solder tails on the PCB landing pad.

## 25.14 – Header, Right Angle Shrouded

**Header, Right Angle Shrouded:** A male multi-pin board connector where the conductive pins are completely enclosed by a four-walled plastic protective casing (the shroud), with the solder tails bent at a sharp 90° angle.

This specific configuration allows external wire harnesses – such as IDC ribbon cables – to plug into the printed circuit board (PCB) parallel to the board surface. This design is heavily favored in space-constrained industrial systems, telecom gear, and computing mainboards to provide maximum mechanical stability and low vertical clearance.



**Structural Anatomy of the Shroud (The "Box")**
Unlike basic unshrouded headers where bare metal pins are fully exposed, the shrouded header surrounds its pins with a rigid, injection-molded rectangular plastic fortress:

- **Four-Wall Protection:** The plastic wall physically safeguards the inner pins against accidental bending, dust, and electrical short-circuits caused by debris or loose wires.
- **The Polarization Slot (Notch):** The center of one long outer wall features a vertical cutout or indentation channel. This slot matches a corresponding plastic key on the female cable socket, physically preventing the cable from being plugged in backwards.
- **Mating Windows:** The interior floor of the shroud often features tiny slots or windows that help center and guide the female terminal contacts during blind mating cycles.

**90° Lead Arrangement and PCB Seating**

- **The Flat-Laying Profile:** The main plastic shroud sits flat and horizontally directly against the top surface of the circuit board.
- **The Right-Angle Solder Tails:** Rigid metal pins emerge from the inner back wall of the shroud, pass through the plastic base, bend exactly 90° downward, and plunge straight through the PCB's plated through-holes to be soldered underneath.
- **Standoff Bosses:** The bottom face of the plastic frame features microscopic molded feet that raise the connector body roughly 0.50 mm off the circuit traces, ensuring cleaning solvents can clear out leftover manufacturing flux.

**Dimensional Standards and Pitch Matrix:** Right-angle shrouded headers adhere to precise, industry-standard grid layouts to ensure global cross-compatibility with external mating harnesses:

- **The Dominant 2.54 mm Matrix:** In standard electronics (like 3M 3000 Series Box Headers), the pins are spaced at a 2.54 mm linear and row-to-row pitch. The individual posts are precision-cut 0.64 mm square metal wires.
- **Sub-Miniature Pitches:** High-density modern computing hardware scales down to tighter standard grids, including 2.00 mm or 1.27 mm pitches.
- **Pin Counts:** Sockets are overwhelmingly manufactured as dual-row (2xN) configurations hosting standardized even pin arrangements such as 10 (2 x 5), 14, 16, 20, 26, 34, 40, or 50 positions.

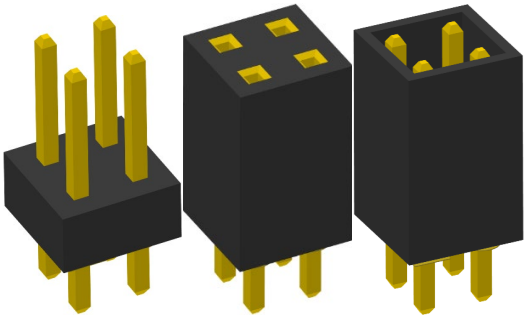
**Specialized Retention Features:** To prevent loose connections in heavy-machinery or high-vibration systems, the outer plastic housing can feature mechanical locking upgrades:

- **Ejector Latches (Long/Short Ears):** Pivoting plastic mechanical arms are often molded onto the two short outer ends of the shroud. When the female connector is pressed inside, these ears click shut to lock it down. Pressing the tabs outward automatically ejects the cable without straining the wire.
- **Friction Lock Ramps:** Smaller pitch headers (like the Molex Micro-Fit 3.0 Series) use an integrated clip ramp on top of the shroud that mechanically snaps into a flexible thumb latch on the wire housing.

## 25.15 – Header, Vertical (All Types)

**Header, Vertical (All Types):** A straight pin header or male header strip) is a board-level connector featuring one or more parallel rows of rigid, completely straight metal pins held uniformly by a plastic insulating strip.

This component is structurally engineered to allow multi-wire cables, daughterboards, or test probes to plug into the printed circuit board (PCB) perpendicular (90°) to the board surface, standing straight up like a tiny metal fence.



**Pin Anatomy and Plating:** The component is constructed using solid, square-cut wire posts (typically brass or phosphor bronze) that are heavily plated with tin, gold, or selective gold-flashing on the mating tips. Each straight pin is physically divided into three zones by its plastic carrier:

- **The Solder Tail:** The shorter end of the pin that passes down through the PCB's plated through-holes to be permanently soldered on the underside of the board.
- **The Insulator Zone:** The middle section of the metal post that is press-fit tightly inside the plastic housing.
- **The Mating Post:** The longer end of the pin that extends straight up into the air, serving as the active terminal that slides into a mating female wire harness or jumper.

**The Plastic Insulator Strip (The "Backbone")**

- **High-Temperature Material:** The pins are held in perfect alignment by a narrow, rigid strip of high-temperature thermoplastic (such as Nylon, PBT, or LCP) capable of withstanding wave soldering or manual iron heat without melting.
- **Breakaway Design (Unshrouded):** On basic unshrouded versions, the plastic strip features small structural notches or score lines between each pin cavity. This allows assembly technicians to easily snap long 40-pin master strips down to any custom pin count needed (e.g., a 3-pin or 5-pin block) with their fingers or a pair of pliers.

**Dimensional Standards and Pitch Matrix:** Vertical post headers strictly follow standardized industrial grids to ensure universal compatibility with third-party jumper wires and test gear:

**The Standard 2.54 mm Pitch:** In the most dominant connector family, the center-to-center linear distance between pins is exactly 2.54 mm. Each metal post has a precise cross-sectional dimension of 0.64 mm square.

- **Sub-Miniature Grids:** Compact consumer electronics utilize tighter standardized configurations, including 2.00 mm, 1.27 mm or 1.00 mm pitches, which feature significantly thinner, more fragile pins.

**Array Configurations**

- **Single-Row (1xN):** A single, straight line of vertical pins.
- **Dual-Row (2xN):** Two identical parallel rows of vertical pins running side-by-side. The linear pitch and row-to-row spacing are identical (2.54 mm x 2.54 mm).
- **Three / Four-Row:** Highly dense blocks used for specialized jumper matrices or legacy backplane systems.

**Assembly and Mounting Features**

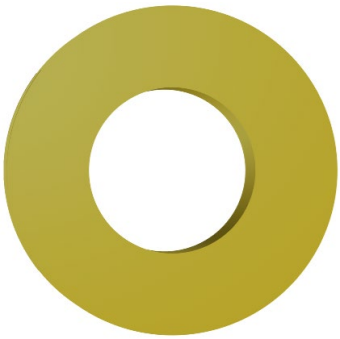
- **Built-In Standoffs:** The bottom face of the plastic insulator strip is molded with tiny feet or a raised channel. This creates a small gap between the plastic and the PCB surface, allowing manufacturing flux gases to escape during soldering and ensuring cleaning solvents can wash underneath.
- **Unshrouded vs. Shrouded:** Unshrouded headers offer the lowest cost and smallest layout footprint but leave pins vulnerable to bending. Shrouded (box) versions enclose the vertical pins inside a four-walled plastic box with a keyway notch to prevent a cable from being plugged in backwards or shifted by one pin.

## 25.17 – Mounting Hole

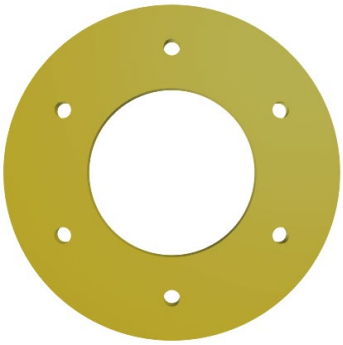
**Mounting Hole:** A precision mechanical feature integrated directly into the substrate of a printed circuit board. Unlike component through-holes, its primary function is structural, allowing screws, bolts, standoffs, or plastic rivets to securely anchor the PCB to an enclosure, chassis, or another circuit board.

Depending on grounding, shielding, and isolation requirements, mounting holes are strictly categorized into two physical styles: Plated (Grounded) and Non-Plated (Isolated). Plated could also include supporting vias.

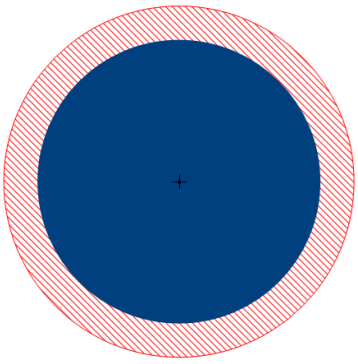
**Plated**



**Plated with supporting vias**



**Non-plated with copper keepout**



**Plated Mounting Holes (Grounded / Chassis Connections):** Plated mounting holes provide simultaneous mechanical fastening and electrical conductivity. They connect the mounting hardware directly to the internal circuitry, typically for chassis grounding or shielding.

- **The Barrel:** The interior wall of the drilled hole is chemically lined with a thin, continuous layer of electroplated copper, creating a conductive cylinder.
- **The Annular Ring Pad:** A circular copper ring surrounds the hole on both the top and bottom layers of the PCB. This copper ring is left unmasked (bare metal without solder mask) and is plated with a surface finish like HASL, ENIG, or tin to provide a smooth, low-resistance contact plane for the screw head or metal standoff.
- **Stitching Vias (The "Via Corona"):** High-reliability or high-frequency designs surround the main hole with a ring of smaller, tightly spaced via holes. This via corona "stitches" the top and bottom copper pads to internal ground planes, reinforcing the barrel against mechanical crushing forces and creating a robust, low-impedance path to shield against electromagnetic interference (EMI).

**Non-Plated Mounting Holes (NPTH / Isolated):** Non-plated mounting holes provide purely mechanical support with absolute electrical isolation.

- **The Barrel:** The interior wall consists of raw, bare fiberglass substrate (FR-4) without any metal plating.
- **The Clearance Zone:** To ensure the metal screw head, washer, or nut does not accidentally bite into nearby traces or cause an electrical short-circuit, a wide keep-out area is strictly enforced. Solder mask covers the surrounding area, and all copper traces, ground planes, and components are swept back outside the physical diameter of the fastening hardware.

**Dimensional Standards and Layout Anatomy**

Mounting holes scale precisely with standard industrial hardware fasteners (such as metric M-series or unified standard #UNC screws):

- **Drill Diameter:** The actual physical hole is drilled slightly larger than the nominal screw size to provide structural clearance and accommodate manufacturing plating tolerances (an M3 screw typically uses a 3.20 mm or 3.50 mm drill hole).
- **The Keep-Out Area:** This defines the total physical boundary reserved for the screw head or assembly tools (like a socket wrench or screwdriver tip). Circuit board designers must leave this circle entirely free of surface components to prevent a screwdriver from slipping and shearing off adjacent resistors or capacitors during enclosure assembly.

**Specialized Variant: Slotted Mounting Holes:** While standard mounting holes are perfectly circular, some high-stress or heavy-duty environments use elongated, oval-shaped slots:

- **The Slot Profile:** A continuous oval channel routed into the board substrate.
- **Purpose:** Slotted holes allow the PCB to slide or shift slightly along a single axis. This manual adjustment window accounts for real-world sheet metal manufacturing tolerances in large enclosures or accommodates thermal expansion and contraction in high-temperature operating environments.

# Appendix I – Referenced Sources

The following sources have been referenced in this Guideline.

*To obtain these documents, click on the document links below:*

**IPC-7352 – Generic Guideline for Land Pattern Design**
*(released 05/2023)*
Footprint Expert's automatic padstack calculations are fundamentally based on IPC-735x formulas and geometry rules. This is the core standard Footprint Expert uses. It defines:

- Land Pattern Naming Conventions for Surface Mount and Through-hole
- Mathematical Model formula for pad stack dimensions
- 3-Tier Density levels for Least, Nominal and Most
- Courtyard Excess toe, heel, and side goals
- IPC-compliant footprint generation rules

**IPC J-STD-001G – Requirements for Soldered Electrical and Electronic Assemblies**
*(released 10/2017)*
This standard influences Solder Joint Goals for Toe, Heel and Side fillet targets.

**IEEE/ANSI 315-1975 – IEEE Standard for Graphic Symbols for Electrical and Electronics Diagrams**
*(released 12/1975)*
Standard Reference Designators

**FED Vol 18 – The New Proportional Land Dimensioning Concepts**
*(released 2018)*
Older proportional land pattern methods influenced the historical development of IPC land pattern standards. Many concepts in the FED Vol 18 evolved into IPC-7351 methodologies.

**IEC_61188-7 – Zero Component Orientation**
*(released 2007)*
This is used for:

- Component orientation conventions
- Zero-degree placement standards
- Assembly documentation consistency
- Pin-1 Orientation A – Pin 1 Upper Left
- Pin-1 Orientation B – Pin 1 Lower Left
- Rotation/origin conventions
- Pick-and-place consistency

**ECIA PDP-100 – Parts Division Publication 100 Registered and Standard Mechanical Outlines for Electronic Parts**
*(released 1987)*

# Appendix II – Guideline Updates

This is the summary of updates to the Guideline since its release.

| | | |
|---|---|---|
| 1.43 | 6/14/2026 | • Typo fixed on page 47: changed “Offset Land Origin” to “Offset Paste & Solder Mask”<br>• Added “om” and “op” on page 47<br>• Updated image on page 35<br>• Structured page 143 Guideline Updates so it is easier to read |
| 1.42 | 6/12/2026 | • Updated images on pages 37 & 59<br>• Reworded several sentences and fixed several typos throughout<br>• Added “Photo Resist” to Terms<br>• Refreshed Table of Contents |
| 1.4 | 6/10/2026 | First completed draft released |

# Appendix III – PCB Footprint Expert Overview

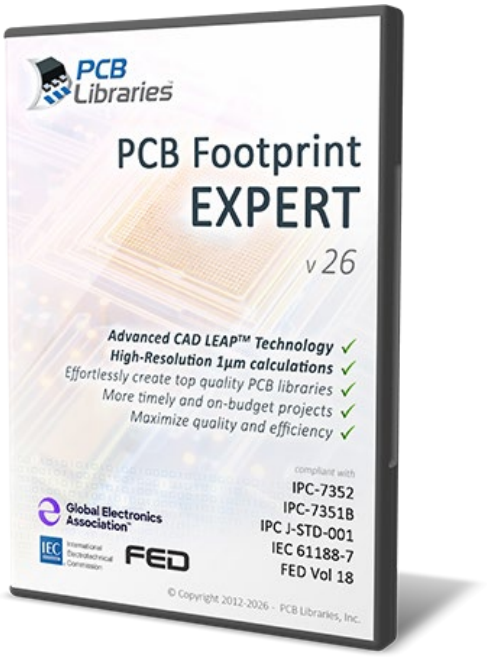
Our completely free **Footprint Calculator** lets you calculate footprints per this guideline. It is available free of charge with registration at https://www.PCBLibraries.com/downloads

Our more powerful **Footprint Expert** automates the attributes of this Footprint Expert Guideline, produces footprints compliant across multiple standards, while allowing flexibility for user-defined requirements, and outputs to 25 CAD formats.

Footprints and 3D component models in this Guideline were automatically generated by the Footprint Expert by using the package dimensions in its built-in calculators.

Footprint Expert users get complimentary access to a starter library of 2 million parts, and free BOM Builder service that matches your part numbers against this database. Any parts we do not have may be outsourced for a nominal fee.

Besides calculator / generator for standard packages, you can also create non-standard footprints using the manufacturer recommended patterns using custom pad stacks




***PCB Footprint Expert*** *automation available from* ***www.PCBLibraries.com***

*high-quality, auto-generated footprints compatible with 25 CAD formats!*

*Get a fully functional evaluation license for any CAD format from* ***www.PCBLibraries.com/Evaluate***